ICSO 2016

International Conference on Space Optics

Biarritz, France

18–21 October 2016

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N. Waltham

Q. Morrissey

M. Clapp

S. Bell

et al.

THE DESIGN AND DEVELOPMENT OF LOW- AND HIGH-VOLTAGE ASICS FOR SPACE-BORNE CCD CAMERAS

N. Waltham, Q. Morrissey, M. Clapp, S. Bell, L. Jones, M. Torbet
STFC Rutherford Appleton Laboratory, Harwell Oxford, Didcot, OX11 0QX, United Kingdom
nick.waltham@stfc.ac.uk

The CCD remains the preeminent visible and ultra-violet wavelength image sensor in space-science, Earth and planetary remote sensing. However, the design of space-qualified CCD readout electronics is a significant challenge with requirements for low-volume, low-mass, low-power, high-reliability and sufficient tolerance to the effects of space radiation. Appropriate space-qualified components that are acceptable to international space agencies are frequently unavailable and up-screened commercial components may not meet project requirements. We have adopted an alternative approach of designing and space-qualifying a series of both low- and high-voltage mixed-signal ASICs to meet these requirements. In this paper we describe our latest ASIC developments including two entirely new high-voltage devices, and our work to upgrade the performance of our earlier devices after many years of successful flight heritage.

A challenging sub-system of any CCD camera is the video processing and digitisation electronics. Our first CCD video ASIC was developed in late 1999 and now has considerable flight heritage in cameras on NASA's Solar Terrestrial Relations Observatory and Solar Dynamics Observatory. In this paper, we describe our more recent developments to improve its performance and radiation tolerance to single event latchup.

Alongside the CCD video processing electronics, the circuitry to generate a CCD's DC bias voltages and drive clocks constitute a significant proportion of a typical CCD camera and present a number of design challenges, exacerbated by the limited range of space-qualified components. To resolve these issues, we have embarked on a programme to develop two high-voltage CCD drive ASICs. Implemented in a 0.35 μm, 50 V tolerant CMOS process, they combine low-voltage 3.3 V transistors that are used within interface logic, voltage reference and digital-to-analogue circuitry, and also high-voltage 50 V diffused MOSFET transistors that can drive a CCD's DC bias and clock electrodes directly.

Our DC bias voltage generator ASIC provides 24 independent and programmable 0-32 V bias outputs. Each channel consists of a 10-bit DAC and a high-voltage output buffer to provide current drive of up to 20 mA into loads of 10 μF, and is current-limited for short circuit protection. An on-board telemetry system featuring a 12-bit ADC and programmable gain buffer allows measurement of the outputs from the bias generators as well as up to 32 single-ended and 4 differential external voltages. One ASIC can drive one or more CCDs directly and replaces an entire PCB of discrete electronics in our current camera electronic systems.

Our clock driver ASIC provides 6 independent and programmable drivers with sufficient current drive for even a large-format CCD's capacitive electrodes. Each driver allows the clock rise-time, fall-time, clock-low and clock-high voltage levels to be programmed independently. It allows the one design to be configured and optimised to drive a CCD's typically 0.1-2 MHz serial readout register clocks or 10-100 kHz imaging area clocks.

Finally, we summarise our future plans and highlight the importance of this technology for developing compact, low-power, high-performance integrated focal plane electronics for the large focal plane array survey telescopes of the future.

I. INTRODUCTION

CCDs are analogue devices that require relatively high drive voltages compared to digital components. Their operation relies on the sequenced pulsing or 'clocking' of multi-phase electrodes to shift the signal charge collected within pixels through the substrate and out to one or more charge detection amplifiers. Low-noise DC bias supplies are required to extract the video signal from the charge detection amplifier(s). Prior to analogue-to-digital conversion, correlated double sampling (CDS) enables the true video signal to be extracted from the output which otherwise contains artefacts from the CCD clocks and reset noise. Significant support electronics are therefore required to read out a CCD sensor and to process and digitise its analogue video signal. The challenges are amplified with the ever increasing aspirations of the space science community requesting ever-larger focal plane arrays of multiple CCDs, reading out at increasingly higher pixel readout rates, and through multiple CCD output amplifiers.

The design of space-qualified CCD readout electronics is therefore a significant challenge with requirements for low-volume, low-mass, low-power, high-reliability and sufficient tolerance to the effects of space radiation. Appropriate space-qualified components that are acceptable to international space agencies are frequently unavailable and up-screened commercial components may not meet project requirements. We have therefore

adopted an alternative approach of designing and space-qualifying a series of both low- and high-voltage mixed-signal ASICs to meet these requirements.

The architectural design of a camera readout electronics system is illustrated in Fig. 1, comprising:

1. Control logic to generate all the timing signals required to read out the CCD, process and digitise the CCD video signal(s), and to convey the data to a data acquisition system.
2. Multiple-phase CCD clock drivers to clock the signal charge out to the charge detection amplifiers.
3. Low-noise DC bias supplies to operate the CCD's output amplifier(s) and charge drains.
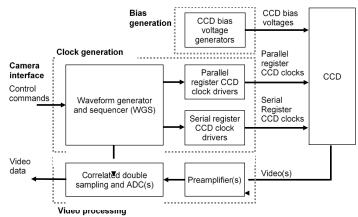4. One or more video preamplifiers, CDS signal processors and analogue-to-digital converters (ADCs).

Fig. 1. Architectural design of a CCD camera readout electronics system

The clock drivers must translate logic-level signals to ~ 10 V amplitude analogue waveforms with sufficient current drive for the CCD's capacitive electrodes. A charge detection amplifier requires several low-noise DC bias voltages of up to ~ 30 V, and provides a video output signal swing ~ 1 V. In the interests of simplification, the need for DC-DC power conversion and secondary voltage regulation is omitted. The following sections describe our development of both low- and high-voltage mixed-signal ASICs to meet these requirements.

II.   CCD VIDEO PROCESSING AND DIGITISATION

A CCD camera's video processing and digitisation electronics is arguably one of the greater design challenges due to the shortage of appropriate high-reliability, low-noise, MHz-rate amplifiers, analogue-switches and high-resolution ADCs that are sufficiently radiation tolerant and, ideally, pre-space-qualified.

In late 1999, these constraints led us to develop our CCD video processing and digitisation ASIC, our first mixed-signal ASIC. We qualified the design for the CCD camera electronics for the Sun Earth Connection Coronal and Heliospheric Investigation (SECCHI) remote-sensing instruments on NASA's twin Solar TErrestrial RElations Observatory (STEREO) spacecraft, launched in 2006 [1,2]. An updated design with greater bandwidth was subsequently developed for the Atmospheric Imaging Assembly (AIA) and the Helioseismic and Magnetic Imager (HMI) remote-sensing instruments on NASA's flagship Solar Dynamics Observatory (SDO), launched in 2010 [3,4].

The architectural design, shown in Fig. 2, consists of an integrated video preamplifier and correlated double sampling (CDS) processor with programmable video offset, a programmable video gain amplifier and a 16-bit ADC [5]. The ASIC has a nominal 1 V signal input range and can operate at up to 2 Mpixels/s. The complete signal chain including the ADC is fully-differential to maximise common-mode noise rejection. A 10-bit DAC enables ±500 mV of programmable DC offset to be introduced into the video signal and a 7-bit programmable x1-x3 gain amplifier enables the ADC to be matched to the CCD signal output swing. The ADC is a 16-bit pipelined converter using feedback capacitor switching in the amplifier stages, and over-ranging at intervals in order to minimise differential non-linearity due to capacitor mismatching and amplifier gain errors. Triple modular redundancy (TMR) is used to enhance the single event upset (SEU) tolerance of the registers.

With its inputs grounded, and configured for unity gain, the ASIC's input referred noise is 46 μV rms (3.0 ADU rms in 16-bits) at 2 Mpixels/s. Connected to an e2v technologies' SDO CCD (CCD203) with an output of 4.5 μV/e-, this equates to an equivalent noise ~ 10.2 e^- rms. The measured integral non-linearity (INL) is ±10 least significant bits (LSBs) and the differential non-linearity (DNL) is ±0.3 LSBs. There are no missing codes within the 16-bit digitisation. The power consumption from a 3.3 V supply is 400 mW.

The ASIC was manufactured on the AMS C35 0.35 μm, 3.3 V CMOS process, known for its excellent tolerance to ionising radiation. Its susceptibility to radiation damage was measured using ESA test facilities. Total ionising dose (TID) tests were made at the Co60 source at ESTEC. Test samples revealed no parametric

changes up to the total test dose of 50 krad(Si), confirming high tolerance to ionising radiation. Single event latchup (SEL) tests were made at the Cyclotron Facility of Louvain-la-Neuve in Belgium using Ne^{4+}, Ar^{8+} and Kr^{17+} ions. The SEL linear energy transfer (LET) profile was examined to 34 $MeVcm^2mg^{-1}$ and the LET threshold was determined to be ~ 14 $MeVcm^2mg^{-1}$. This was lower than expected and less than the SDO minimum LET threshold requirement. The four video ASICs within the SDO camera electronics were therefore individually protected with current-sense circuitry to detect a sudden increase in supply current and a current-trip to inhibit the supply. Further SEL testing showed that nominal operation could be restored by power-cycling the ASIC. Two samples were subjected to, and shown to recover from ~ 200 SEL-induced events each, suggesting that destructive SEL would be rare.
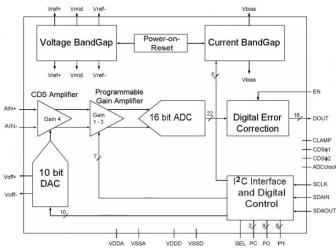

Fig. 2. Architectural design of the CCD video processing ASIC

Further design iterations and optimisation of the SDO video ASIC has led to a modest reduction in readout noise, reduced signal settling time and increased linearity. However, our most significant development has been to harden the ASIC's susceptibility to SEL.

Hardening of CMOS circuits against SEL can be achieved by the inclusion of 'guard-rings' within the chip layout. The physical process of an SEL involves the same parasitic silicon controlled rectifier (SCR) circuit responsible for electrically induced latchup. Transient current flow from an energetic particle must flow through the n-well or substrate to a supply contact to be discharged. The resistance of this path can generate a voltage drop which, if sufficiently large, can turn on the base-emitter junction of a parasitic bipolar junction transistor, in turn activating the SCR and shorting the power supplies. In a hardened design, continuous rings of substrate and well contacts are placed around transistors and wells to provide the transient current with an alternate low-resistance path to a supply rail. These low-resistance paths greatly increase the current, and therefore the energy that an energetic particle must deposit to turn on the SCR. In the case of the AMS C35 CMOS process, these guard rings need to include metal strapping to achieve sufficiently low-resistance.

A new version of our CCD video processing ASIC has been designed and fabricated with SEL-resistant guard-rings using a custom-developed cell library. We are currently in the process of sub-contracting ASIC packaging, screening, qualification and radiation testing. However, our most recent DAC ASIC was also designed with the same cell library and has been SEL tested. Results are presented below and lead us to believe that our new video ASIC will be SEL-immune.

III. CCD DC BIAS

A CCD requires a number of low-noise DC bias supplies to operate its output amplifiers and charge drains. The output amplifiers typically require supplies of up to 30 V. Careful optimisation of these bias voltages can help minimise readout noise and maximise charge-handling capacity. The ability to software-program and adjust these bias voltages is clearly desirable.

For the SDO cameras, we developed and space-qualified a programmable 8-channel digital-to-analogue converter (DAC). The architectural design, shown in Fig. 3, consists of eight 10-bit programmable voltage-output DACs [5]. Each DAC consists of an input register, a DAC register, a resistor ladder, and a multiplexer connecting the appropriate tap from the resistor ladder to a voltage output amplifier. The input registers and DAC registers provide double buffering. TMR is used to enhance the SEU tolerance of the registers. Data programmed into the input registers can be transferred into the DAC registers independently or collectively under the control of an external load-enabling clock. Each DAC contains a resistor ladder of 1024 series-connected 100-ohm resistors. The 10-bit DAC code determines the resistor ladder tap that is fed through

to the output amplifier. The design is guaranteed to be monotonic. The output voltage range is set by an external voltage reference of 2.5 V. An output-enabling function allows all DACs to be enabled or disabled collectively. A power-on-reset circuit ensures that all DACs are initialised to 0 V.

Within the SDO camera electronics, the ASIC provides six programmable voltages in the range 0 V to 2.5 V. These add an offset voltage to a set of low-noise operational amplifier (op-amp) ICs configured to provide the minimum necessary CCD biases set through resistor potential dividers. The minimum biases did not need to be set critically as the intention was always to add a little more offset voltage via the DACs. We could therefore eliminate the necessity to test and adjust select-on-test resistors on flight printed circuit boards (PCBs). This ASIC was also radiation tested. We obtained similar results to our video ASIC for TID radiation, but slightly better results for SEL for which the LET threshold was determined to be ~ 20 MeVcm^{2}mg^{-1}.

A new version of our DAC ASIC has also been fabricated with SEL-resistant guard-rings using the same custom-developed cell library that we used for our new CCD video processing ASIC. We again used the Cyclotron Facility of Louvain-la-Neuve and examined the SEL LET threshold to 135.4 MeVcm^{2}mg^{-1} using Ne^{4+}, Ar^{8+}, Kr^{17+} and Xe^{26+} ions. Numerous SEU events within the registers were identified when the TMR reset-logic was purposely disabled. However, no SEL events were detected, verifying that our guard-ring technology is effective with a SEL TID threshold now greater than 130 MeVcm^{2}mg^{-1}.
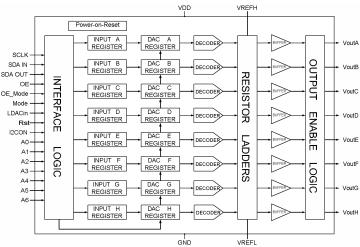

Fig. 3. Architectural design of the low-voltage DAC ASIC

The low-voltage outputs of our DAC ASIC were clearly a limitation, necessitating additional external op-amps to establish the 0-30 V biases. We therefore decided to design a more ambitious ASIC exploiting the 50 V high-voltage diffused MOSFET (DMOS) transistors offered on the AMS 0.35 μm H35 process. This process would enable 3.3 V transistors used within the interface logic, voltage reference and DACs to be combined with 50 V DMOS transistors that could provide a CCD's high-voltage bias supplies directly. The low-voltage circuits would operate from a 3.3 V supply while the high-voltage outputs would operate from a 35 V supply. However, as with many multi-rail electronic components, the application or removal of these supplies needs to be managed. Specifically, the high-voltage positive supply must always remain higher than the low-voltage positive supply to prevent forward biasing of parasitic bipolar junctions.

The Space Telemetry And Reference (STAR) ASIC is a complete high-voltage CCD DC bias voltage generator that integrates 24 independent and programmable low-noise 0-32.736 V voltage-output DACs with on-chip voltage and current references and a multi-channel 12-bit ADC housekeeping telemetry system [6]. One ASIC can drive one or more CCDs directly and replaces an entire PCB of discrete electronics in our current camera electronic systems. The architectural design is shown in Fig. 4.

Each DAC consists of a 10-bit segmented resistor-string monotonic DAC and a high-voltage output buffer that provides current drive of up to ±20 mA into loads of 10 μF and with ±25 mA current-limiting short-circuit protection. The input to each DAC is an individually buffered 2.048 V reference derived from a master on-chip bandgap voltage reference. The resistor-string provides an output in the range 0-2.046 V in 2 mV steps. A high-voltage class AB differential input op-amp with x16 gain amplifies this to provide the required 0-32.736 V output range in 32 mV steps. Since intended to provide only DC bias voltages, the amplifier is compensated to limit its bandwidth to 60 kHz and thus minimise noise. Output noise is a function of capacitive load, decreasing from < 100 μV rms with negligible capacitive loading, to an output voltage dependent 20-40 μV rms with 10 μF loading [6]. The DAC's amplifier gain is accurate to < 0.3% and the zero-offset voltage is < 1 LSB (32 mV). The measured INL is typically < 0.6 LSBs and the DNL < 0.2 LSBs. Running from a 35 V supply, each DAC's quiescent power consumption is 28 mW.

The housekeeping telemetry system enables monitoring of the 24 high-voltage DACs and up to 32 single-ended and 4 differential off-chip voltages. The differential inputs are intended for reading platinum resistance temperature sensor Wheatstone bridge circuits. The telemetry system consists of an analogue multiplexer, a differential input variable gain amplifier, and a 12-bit successive approximation register ADC. The multiplexer includes 16:1 resistive dividers on its inputs where appropriate for scaling high-voltage signals to match the 2.048 V input range of the ADC. The ADC operates at up to 667 kHz (samples per second). Characterisation confirmed an INL typically < 1.3 LSBs, a DNL < 0.5 LSBs, and sample noise < 0.75 LSBs rms.

The ASIC is controlled through a 3.3 V CMOS logic-level Serial Peripheral Interface (SPI) bus. All registers are TMR protected against SEUs and guard-rings are used throughout the design to protect against SEL.

With the exception of the bandgaps, some biasing circuits, and the power-on-reset circuit, each of the ASIC's sub-systems has a power-down mode to enable unused circuits and channels to be disabled to save power if not required. The ASIC powers up in the minimum power state with only the bandgaps and basic biasing circuitry active, and with a power dissipation of 37 mW. The DACs and telemetry circuits can then be enabled individually with the power dissipation increasing to 1.17 W with all circuits active and all DACs driving 32.736 V outputs.

Designed and fabricated on the AMS 0.35 μm H35 CMOS process, the finished die size is 15.12 mm x 13.95 mm and intended for encapsulation in a 144-pin CQFP package. For initial evaluation and characterisation, an unpackaged die was mounted on a purpose-designed carrier PCB. A National Instruments PXI crate fitted with appropriate analogue and digital I/O modules was used to drive the ASIC and measure the DAC outputs [6]. The H35 process design kit allows simulation over a temperature range of -40°C to 125°C and therefore the ASIC was also characterised over this range. The now successful completion of this testing provides confidence to embark on a campaign of die packaging, screening, qualification and radiation testing.
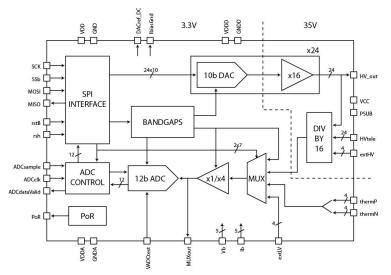

Fig. 4. Architectural design of the high-voltage CCD DC bias ASIC (STAR)

IV. CCD CLOCK DRIVING

Finding sufficiently high-speed, space-qualified, or adequately reliable and radiation-tolerant ICs that can drive a CCD's capacitive electrodes is a further challenge. The clock drivers must translate logic-level signals to high-current drive waveforms ~ 10 V amplitude as illustrated in Fig. 5. Varying drive frequencies are required, ranging typically ~ 0.1-2.0 MHz for a science-grade CCD's serial register readout clocks, and ~ 10-100 kHz for its imaging area, or parallel register readout clocks. The loading that the drivers will see also varies, ranging typically ~ 50-200 pF for a CCD's serial registers phases, and ~ 10-100 nF for its parallel registers phases. In practice, a CCD load is more complex than a simple capacitive load, and represented better by a lumped RC model which also accounts for electrode resistance and adjacent electrode phase capacitance as well as the capacitance to substrate. Waveform rise-time, fall-time and clock-phase overlap are also essential considerations in determining and maximising a CCD's charge transfer efficiency. A further factor is distortion of the drive clocks from adjacent electrode phase capacitance, so-called interphase coupling effects. Fig. 5 illustrates how parameters can be placed on these issues in order to define requirement specifications.

For compactness, many designers rely on MOSFET driver ICs, but these are often compromised in one or more aspects of speed, space-qualified packaging and/or reliability, or radiation tolerance requirements. Many projects are obliged to undertake comprehensive and expensive up-screening, qualification and radiation testing

campaigns of commercial components. Our solution has been to design our own mixed-signal, high-voltage CCD clock driver ASIC. The architectural design is shown in Fig. 6.

The CCD Clock Buffer ASIC (C2BA) was designed to drive e2v technologies' science-grade CCDs. It provides 6 independent and programmable clock drivers with sufficient current drive for even a wafer-scale CCD's parallel register capacitive electrodes. Each driver allows the CCD clock-high and clock-low voltage levels as well as the constant-current slew rates of the clock-rise and clock-fall transitions to be programmed independently.
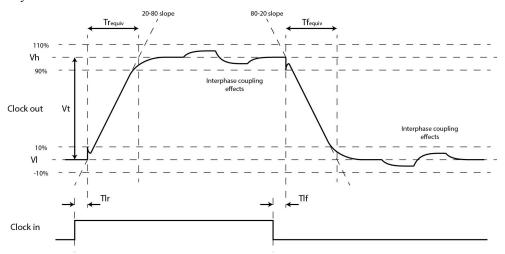

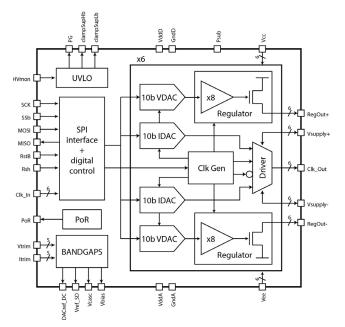**Fig. 5.** CCD clock driver waveform definition

Fig. 6. Architectural design of the CCD clock driver ASIC (C2BA)

Each clock driver consists of a pair of programmable voltage regulators, a pair of programmable current sources and a switched current driver. The driver charges and discharges the output node with constant currents operating between the two voltages set by the regulators.

The voltage regulators are controlled by voltage-output DACs and are used to set the clock-low (Vl) and clock-high (Vh) voltages in the range 0-16.368 V. Each DAC consists of a 10-bit segmented resistor-string fed from a buffered 2.048 V voltage reference, the same design as used in the STAR ASIC. The output of the DAC is fed into a high-voltage op-amp with x8 gain to provide the required 0-16.368 V output range in 16 mV steps. The output of this op-amp is fed to a unity gain output stage which provides high load current handling capability. This circuit is configured to source or sink current as required with a very fast response time, enabling the regulators to handle the high-speed changes in load current needed to produce sub-100 ns clock edges, and also accept reverse current flow back into the regulator caused by interphase coupling effects in the CCD load. The circuit will accommodate off-chip decoupling capacitors of up to 1 μF for noise reduction

though does not require them for stability. On power-up all voltage regulators are disabled and operate at minimal bias current with outputs ~ 0 V. Each regulator is then programmed to be enabled or left disabled.

The two programmable constant-current sources allow the slew rates of the clock-rise (Tr) and clock-fall transitions (Tf) to be set independently and generate linear clock transitions. In practice, linearity is defined across the 20-80% clock swing transition region, as illustrated in Fig. 5. Our design goals required Tr and Tf to be programmable from 20 ns to 20 µs, and the output driver to be stable operating into capacitive loads from 2 pF to 200 nF. The driver was also required to have fixed propagation delay between the logic-level input clock and the start of the output driver's clock swing, Tlr and Trf in Fig. 5, and independent of Tr and Tf. Interphase coupling effects were specified to be < ±10% of the clock swing amplitude (Vt) and the output noise was to be < 100 µV rms on settled waveform outputs.

The input to the switched current driver consists of a pair of 10-bit binary-weighted current DACs designed to provide output currents between an LSB of 250 nA and a maximum of 256 µA. These are fed into multiplying current mirrors with x1600 gain to increase the maximum drive current to ~ 400 mA. A clock generator controls the circuitry from the logic-level input clock. On power-up all the clock drivers are disabled, operating with minimal bias current and the outputs tri-stated (high impedance). Each driver is then programmed to be active or left inactive.

The ASIC is controlled through a 3.3 V CMOS logic-level SPI bus, similar to that of the STAR ASIC. All registers are TMR protected against SEUs. A refresh pin enables the TMR register states to be refreshed or corrected independently of whether the interface is being clocked. Guard-rings are used throughout the design to protect against SEL. The ASIC incorporates updated versions of the voltage and current bandgaps used in the STAR ASIC.

Due to the physical structure of the high-voltage DMOS transistors implemented in the AMS H35 process, care must be taken to ensure current flows in the correct direction for each device type. Unlike conventional low-voltage FETs, the high-voltage FETs must only conduct current from drain to source for NMOS devices and from source to drain for PMOS devices. Driving current the wrong way through a device turns on parasitic bipolar elements and dumps large currents into the substrate, risking direct damage to the device or triggering latchup. The ASIC therefore incorporates additional circuitry to protect against such an occurrence, either due to direct user action or through unforeseen events such as an outage on the power supplies. The operation of each driver is controlled by a finite state machine to ensure controlled power sequencing of the components from power-up or during power-down. It ensures that the voltage across, and current flow through, the high-voltage DMOS transistors is always of the correct polarity. All channels start in standby mode. Clocking up or down the state machine is managed through the SPI bus with dedicated commands. Safe shutdown of the ASIC from inadvertent power loss is managed by an asynchronous analogue protection system. This consists of an under-voltage detection and lockout (UVLO) circuit which shuts down the high-voltage regulators and drivers in the correct sequence to avoid damage to the ASIC.

Designed and fabricated on the AMS 0.35 µm H35 CMOS process, the finished die size is 11.1 mm x 11.1 mm and intended for encapsulation in a 132-pin CQFP package. For initial evaluation, an unpackaged die has been mounted on a purpose-designed carrier PCB in a similar scheme to that used to test the STAR ASIC. A National Instruments PXI crate, again fitted with appropriate analogue and digital I/O modules, has recently been commissioned for characterising the ASIC over the temperature range -40°C to 125°C. We are still in an early phase of testing, but results so far are encouraging. To date we have confirmed that all chip sub-systems function correctly. Oscilloscope traces of the drivers working into loading networks that are representative of typical CCD loads are reproduced in Fig. 7.
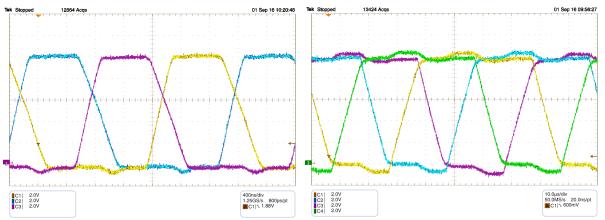

Fig. 7. Serial (left) and parallel (right) register clock waveforms into representative loads

On the left is a trace of 3-phase serial clock drivers working into loads of 120 pF to substrate (0 V) and 140 pF interphase coupling capacitance. The clock amplitude has been set to 10 V and the clocking frequency to 1 MHz. The clock phase overlap has been set to ~ 60% which gives rise to the small interphase coupling seen on the clock-lows. On the right is a trace of 4-phase parallel clock drivers working into more substantial loads of 70 nF to substrate and 16 nF interphase coupling capacitance. The clock amplitude has been set to 10 V and the clocking frequency to 12.5 kHz, or a line-transfer time of 80 μs. Interphase coupling effects are more evident as we expect, but $< \pm 10\%$ of the clock swing amplitude as specified. More comprehensive testing will include characterising the drivers operating into a full range of minimum, typical and maximum loading networks with appropriate minimum, typical and maximum clock slew rates, clock-high and clock-low voltage levels, and clocking frequencies.

V. CONCLUSIONS AND FUTURE PLANS

We have described our programme of both low- and high-voltage mixed-signal ASICs development for the control and readout of space-borne CCDs. With the addition of a radiation-tolerant FPGA to provide logic-level camera control, waveform generation, timing and external communication, we now possess a unique set of building blocks for the assembly of compact, low-mass, space-qualified CCD camera electronics systems.

We have successful flight heritage of our low-voltage CCD video processing and DC bias DAC ASICs through the CCD camera electronics we developed for NASA's STEREO and SDO missions. Our new high-voltage ASICs provide highly-integrated and programmable multi-channel CCD clock drivers and low-noise DC bias supplies that can interface directly with, and provide the drive for e2v technologies' CCDs. Our 6-channel CCD clock driver ASIC enables independent control of each channel's CCD clock-high and clock-low voltage levels as well as the constant-current slew rates of the clock-rise and clock-fall transitions. Our 24-channel high-voltage CCD bias voltage ASIC has sufficient outputs for more than one CCD and also incorporates a multi-channel housekeeping telemetry system.

The next challenge to consider is the packaging and qualification of the ASIC die. So far we have followed a conventional route of assembly and space-qualification of individual die in standard CQFP packages. We will continue to pursue this route for our conventional camera electronics designs. However, for more challenging applications, we will also explore multi-die hybrid packaging technologies (multi-chip modules). The attractions are greater compactness and anticipated savings in packaging and qualification costs. The disadvantage is that these modules can become overly-custom, application-specific and carry a concern of impractically high power density. With increasing compactness, power dissipation, and thermal management may become the next significant design drivers.

With the increasing sophistication of space-borne CCD camera systems, more frequently calling for large focal plane arrays of tiled CCDs with multiple video output ports, the benefits of highly-integrated ASIC functionality and high-density packaging become increasingly attractive and necessary. We believe we already have some valuable building blocks and a strategic development programme to meet the needs of these ambitious programmes.

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