Design of high precision ring ICO circuit with power supply voltage of 0.77V in 0.18μm CMOS process

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ABSTRACT

In this study, a circuit structure of ring current controlled oscillator (ICO) is proposed. Through the cooperation of counter, bootstrap switch with special timing control and special ICO circuit module, the output frequency accuracy in traditional ring OSC is avoided from being affected by voltage range limitation and comparator delay, the temperature and voltage characteristics of output clock are improved, and the output clock with higher accuracy is obtained under low voltage and low power consumption. The test chip is manufactured by 0.18 μm CMOS process. The power supply voltage is 0.77 V, and its output frequency is 1.32 MHz. The deviation of the output clock with the power supply voltage is within ± 1%, the deviation with the temperature is within ± 2.5%, and the power consumption is 382 nW.

Keywords: ICO, OSC, low voltage, low power consumption, high precision

1. INTRODUCTION

Oscillator (OSC) is an important part of many electronic systems and is widely used in various electronic devices[1, 2]. With the expansion of application scope and the development of integrated circuit, the demand for high-performance OSC circuit is higher and higher, which has also become an important research topic[3]. The design difficulty of OSC circuit lies in the balance and compromise of many performances such as low voltage, high precision and low power consumption[4, 5]. Ring oscillator has become the most commonly used structure because of its feedback regulation, relatively high precision and simple implementation[6].

In the existing ring OSC circuit, because the clock cycle is related to the delay, and the delay is greatly affected by the process and temperature, resulting in large frequency deviation[7], poor stability and low circuit accuracy, which cannot fully meet the requirements of the system for high-performance OSC circuit. Generally, in P, T and V simulation, it is difficult to control the output frequency deviation of OSC within ± 10%, let alone ± 5%. Based on this, a low-voltage, low-power and high-precision ring ICO circuit structure is proposed in this paper.

2. TRADITIONAL RING VOLTAGE CONTROLLED OSCILLATOR CIRCUIT

As shown in Figure 1, the traditional ring voltage controlled oscillator (VCO) mainly includes current source circuit, RC circuit, operational amplifier circuit (OPA), VCO and other circuit structures[8]. Its main working process is as follows: the current source provides currents $IBIAS_1$ and $IBIAS_2$ for RC circuit and OPA respectively; The resistance R branch in the RC circuit provides the reference voltage V_R for the lower OPA; The capacitor C branch completes the charging and discharging process alternately under the control of the ordinary switch, and takes the voltage on it as the input V_C at the other end of the OPA; The voltages V_R and V_C are differentially amplified by the OPA to obtain the voltage V_0; In VCO, the output clock signal F_{out} is converted; In addition, the output clock will feed back to control the operation of the current source and RC circuit, so as to realize the circuit feedback control[9]. The frequency value is:

$$f_{out} = A_V K_{VCO} I_{ref} (R_{out} // C_{out}) (\frac{dZ_{vin+}}{df_{out}}) = A_V \frac{\frac{1}{sC_{out}}}{R_{out}+\frac{1}{sC_{out}}} K_{VCO} I_{ref} (-\frac{C_2}{(sC_{in}+\frac{1}{R_{ref}})^2}) \quad (1)$$

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In the above equation, $(\frac{dZ_{vin+}}{df_{out}})$ refers to changing frequency into impedance, A_V is the gain of OPA, K_{vco} is the parameter of changing voltage into frequency, and C_{in} is the voltage stabilizing capacitor of RC branch; R_{out} and C_{out} are the output resistance and output capacitance of the OPA, and have: $\Delta V * K_{VCO} = \Delta f$ [9].

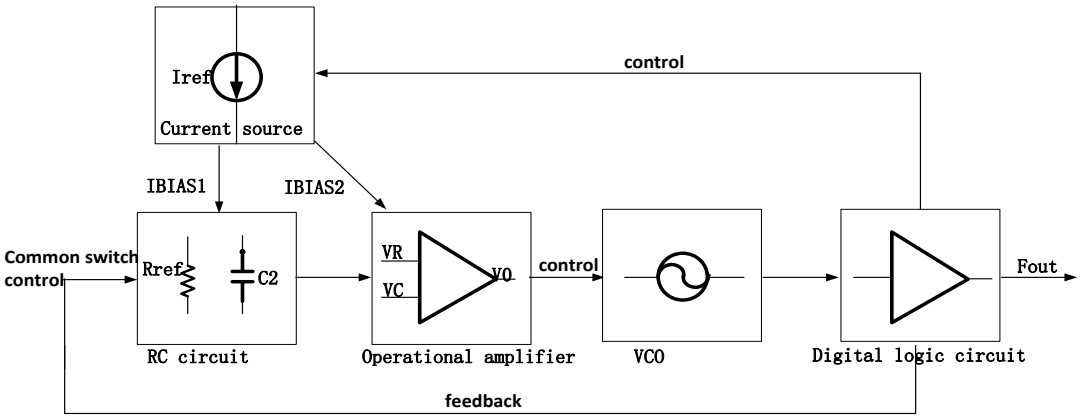

Figure 1. Traditional ring VCO architecture.

Under the starting state and normal working state of this circuit, the current demand of the system is different, and the working condition of MOS transistor is different. If it is not distinguished, the power consumption and accuracy performance of the circuit will deteriorate; Secondly, the common switch controlled by the digital logic circuit will have the risk of leakage, and in the VCO circuit, when the power supply voltage is low, the output voltage range of the OPA is narrow, resulting in the limited output frequency range of the circuit, which will seriously deteriorate the accuracy of the system and even cause the circuit to stop vibration. To sum up, this circuit has defects in accuracy, power consumption and other performance.

3. HIGH PRECISION ICO CIRCUIT

3.1 Overall architecture

Based on the traditional ring VCO circuit, the structure proposed in this paper introduces circuit modules such as bootstrap switch, counter and specially designed ICO controlled by special timing, so as to greatly improve the circuit performance and make it can be used in low-voltage, low-power and high-precision places. The specific architecture is shown in Figure 2, the current source acts on the resistance to form the reference voltage V_R, and $V_R = I_{ref} * R_1$. On the other hand, the current source charges capacitor C_2 to form voltage V_C. C_1 and C_3 are voltage stabilizing capacitors. Its working process is: When $V_R > V_C$, the charge obtained by the capacitor C_2 through the current source is less than the charge discharged by the circuit through the capacitor C_2, the output voltage of the OPA decreases, the current value obtained by ICO decreases, the charging time of the circuit becomes longer, and the output clock frequency decreases. After circuit feedback, the on-off frequency of the Control RC circuit decreases, and more charge will be charged on the capacitor C_2, which increases V_C and plays the role of negative feedback; Similarly, when $V_R < V_C$, the charge obtained by the capacitor C_2 through the current source is greater than the charge discharged by the circuit through the capacitor C_2, the output voltage of the OPA increases, the current value obtained by ICO increases, the charging time of the circuit shortens, and the output clock frequency increases. Through the circuit feedback control, the switching frequency of the RC circuit increases, and the charge charged on the capacitor C_2 will decrease, thus reducing V_C. The circuit constantly changes between these two states to form a stable clock signal. Here, the amount of charge obtained by C_2 from I_{ref} is equal to the amount of charge released from C_2, i.e.:

$$I_{ref} * t = C_2 * V_R \tag{2}$$

Thus there:

$$t = \frac{C_2 * V_R}{I_{ref}} = C_2 * R_1 \tag{3}$$

$$f = \frac{1}{t} = \frac{1}{C_2 * R_1} \tag{4}$$

So the values of C_1 and C_2 can be calculated; The resistance with the smallest deviation with temperature change is constructed by temperature compensation, and the capacitance with the best temperature coefficient is used as C_2, and the device with the largest unit capacitance is used as C_1.

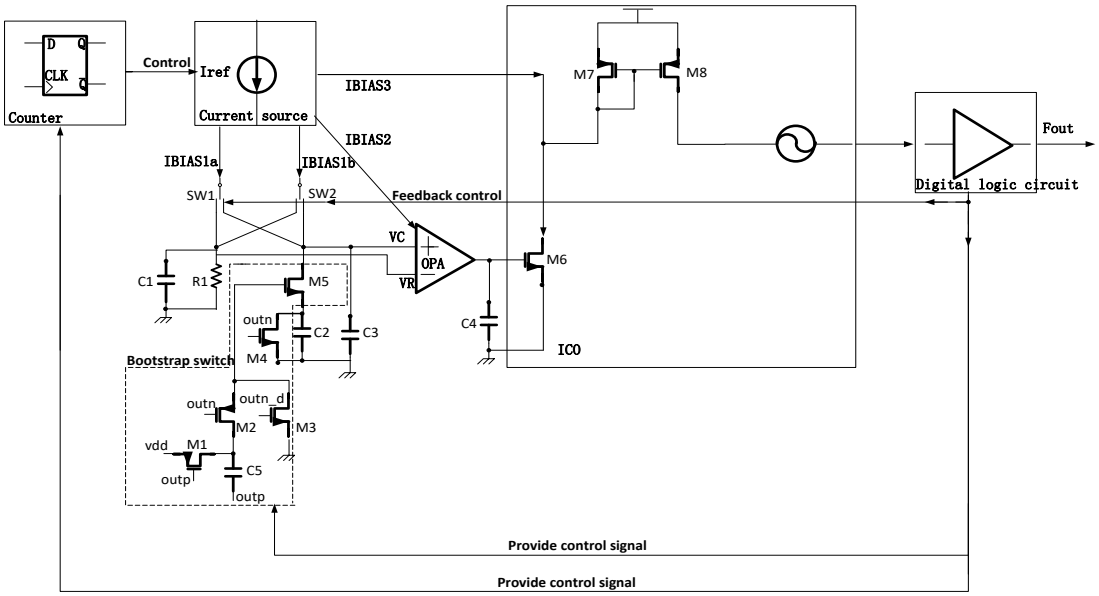

Figure 2. High precision ring ICO circuit architecture.

The OPA uses a common source and common gate structure, and the offset needs to be considered in the design process. In order to enhance the loop stability of the circuit, the gain value of the circuit needs to be controlled reasonably; Considering the reasonable size of input tube and load tube, the gain value of input tube must be greater than that of load tube.

In this circuit, a counter is introduced to control the operation of the current source module. In the initial stage of the circuit, a relatively high bias current is provided for the OPA to reduce the establishment time of the OPA, and reduce the current after the normal operation of the circuit, so as to reduce the power consumption; By adopting the bootstrap switch circuit controlled by special timing, the accuracy of the circuit will be greatly improved and the circuit can work at a lower power supply voltage; In addition, the output frequency range of the circuit is widened through ICO structure to improve the accuracy and speed of the circuit.

3.2 Design of counter

The counter circuit is composed of D flip-flop. Its main function is to count the output clock of OSC to realize the delay function. As shown in Figure 2, on the one hand, the counter controls the current source to reduce power consumption, on the other hand, it controls the operation of switch SW_1 and switch SW_2 to increase speed and accuracy.

Firstly, the counting result will control the output current value of the current source circuit and provide large current to the OPA at the beginning of power on, so as to meet the demand for large current when the feedback loop looks for and adjusts the circuit working point, so as to reduce the loop stability time. After the circuit works stably, that is, after the counting is completed, the demand for large bias current of the whole circuit decreases, and then reduce the output value of the current source, so as to reduce the power consumption.

Secondly, during normal operation, the current sources $IBIAS_{1a}$ and $IBIAS_{1b}$ alternately provide current for the branches where R_1 and C_2 are located under the control of switch SW_1 and switch SW_2 to realize the chopping function. The chopping structure of the current source is used to eliminate the influence of the difference between the current sources $IBIAS_{1a}$ and $IBIAS_{1b}$ on the output frequency. However, if the capacitor charging process is not over, the two current sources are exchanged, which will introduce the error of the capacitor branch into the resistance branch and reduce the

circuit accuracy. Because before V_C is not stable, the current in the branch where resistor R_1 is located is different from that in the branch where capacitors C_2 and C_3 are located, and the current source tube supplying power to C_2 and C_3 branches initially works in the unsaturated area. At this time, the current of C_2 and C_3 branches is 0 and the current of R_1 branch is $IBIAS_1$. At this time, if the current sources of two branches are exchanged, a transition period will occur and the voltage V_R on the resistance will be unstable, and V_R is used as the reference voltage of the whole circuit. If instability occurs, it will eventually lead to the instability of the whole loop, which will seriously affect the accuracy of the circuit. In addition, the power on speed of the OPA is often slower than the charging speed of the RC circuit. If special treatment is not carried out, the working state mismatch will occur among the current source circuit, RC circuit and OPA. Therefore, the structure controls the working conditions of switch SW_1 and switch SW_2 through the counter, so that the circuit nodes will not exchange current sources before reaching the working voltage, so as to avoid the power on error of each branch of the circuit, especially the capacitor branch and OPA, being introduced into the OSC and affecting the accuracy of the whole circuit.

3.3 Design of bootstrap switch

The bootstrap circuit uses the characteristics of capacitor storage charge to realize boost. As the core circuit of the OSC, C_2 branch in Figure 2 is very sensitive to leakage, so the conductivity and leakage of the control switch will be very helpful to improve the circuit accuracy and reduce the circuit power consumption. This structure uses the special timing control signal shown in Figure 3 to assist the operation of the bootstrap switch, which can not only improve the accuracy of the circuit, but also make the circuit work at a lower power supply voltage.

Figure 3 shows the three control signals outn_d, outn and outp timing diagram, in this way, multiple complementary overlapping clocks can be constructed. The specific working process is as follows: in Figure 2, in the first half cycle, outp= 0, outn= 1, outn_ d= 1, M_1 tube is on, M_2 tube is off, M_3 and M_4 tube is on, M_5 tube's gate voltage is 0, M_5 tube is off, and M_2 tube's drain voltage value is V_{DD}; In the second half of the cycle, outp= 1, outn= 0, outn_ d=0, M_1 tube turns off, M_2 tube turns on, M_3 and M_4 tube turns off. Under the action of C_5, the gate voltage of M_5 tube is $V_{gM5} = V_{DD}$ + outp, which improves the conductivity of M_5 tube. Using multiple complementary overlapping clocks and working with the bootstrap switch in the design can not only reduce the overshoot and improve the continuity of the switch, but also ensure that M_4 tube and M_5 tube will not be connected at the same time, so as to reduce the frequency deviation caused by the additional discharged charge due to leakage and improve the accuracy of the OSC.

3.4 Design of ICO circuit

Figure 4 shows, the gate voltage V_{IN} of M_6 is the output voltage of the OPA. C_4 filters this voltage to reduce interference. During operation, I_{M6} changes with the change of V_{IN}, and through the current mirror image of M_7 and M_8 tube, together with the current $IBIAS_3$, finally forms the current of M_9 tube $I_{M9} = I_{M6}$ - $IBIAS_3$. Thus, the transformation from voltage to current is realized, and then the current is transformed into output clock by controlling the operation of the ring inverter with this current.

Although the output range of the OPA is narrow, the current range that can be controlled is very wide, so the current range supplied to the ICO circuit is very wide, which widens the output frequency range of the circuit and makes it match the frequency range corresponding to the previous RC circuit, which greatly improves the accuracy of the system; On the other hand, the introduction of current source makes the current of the whole circuit limited and the power consumption controllable. In the design, it is necessary to consider the matching of g_m of M_6 and the later $IBIAS_3$ on the control ability of frequency F, that is, the ability to change from V_{IN} to $IBIAS_3$ and from $IBIAS_3$ to F need to be matched with each other, otherwise the stability and regulation ability of the loop will be affected.

Figure 4 shows, its core components are the ring inverter composed of an odd number of inverters whose current is controlled by I_{M12} and I_{M13}, and the output circuit for shaping. When the frequency is high, the range of voltage V_B at the output terminal B of the ring inverter is not V_{DD}-V_{SS}, but V_1-V_2, and $V_{SS} < V_2 < V_1 < V_{DD}$. Ideally, M_{12} tube and M_{13} tube are completely symmetrical, and V_1-$V_{SS} = V_{DD}$-V_2. However, in the actual design, V_B is very sensitive to mismatch, and the offset will lead to the deviation of V_B voltage range, resulting in the non operation of M_{16} and M_{17}. In order to solve this problem, on the one hand, $W_{M13} = 2W_{M12}$ is set in this structure, so that $I_{M12} \neq I_{M13}$, that is, the influence of device mismatch on the circuit becomes insignificant by deliberately pulling the working state sharply, so as to eliminate the influence of offset on the circuit. At this time, the voltage range of V_B shifts towards V_{SS} as a whole. In addition, because the circuit is no longer sensitive to mismatch, the size of each tube in this module can be relatively small to reduce the circuit parasitic, so as to further improve the circuit accuracy. C_6 is used to realize voltage stabilizing and filtering.

On the other hand, capacitor C_7 is introduced to improve the working state of M_{16} and M_{17} tube and improve the circuit accuracy. Capacitor C_7 can not only realize isolation and prevent the jitter of clkout end from being coupled to the gate of M_{16}, so that the gate voltage between M_{16} tube and M_{17} tube is relatively independent; It can also complete the charge transfer, superimpose V_B on the DC level, improve the conductivity of M_{16} tube, improve the inconsistency of M_{16} and M_{17} conductivity caused by the overall downward deviation of V_B, improve the duty cycle of Vout and reduce the design difficulty of M_{16} tube and M_{17} tube. Among them, for V_A:

$$V_A = \frac{Z_L}{Z_L+Z_C} V_{in} = \frac{V_{in}*Z_L*jwC}{(Z_L*jwC)+1} \tag{5}$$

From equation (5), it can be seen that when the coupling capacitance increases, Z_C decreases, resulting in the increase of V_A. the final design takes the coupling capacitance as 320fF. In addition, the current source provides bias for point A. on the one hand, it provides DC level for point A, on the other hand, it makes its current value change synchronously with the system, so as to ensure the smooth progress of loop regulation process.

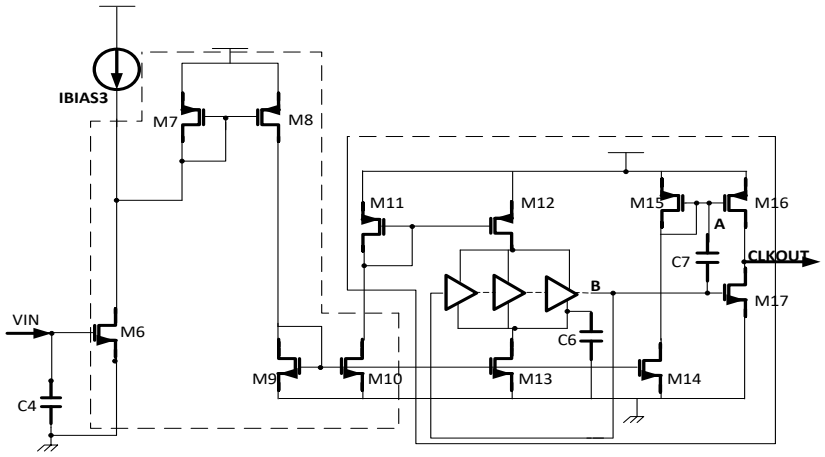

Figure 4. Schematic diagram of ICO circuit.

3.5 Summary

In short, the three circuit modules of counter, bootstrap switch controlled by special timing and ICO are indispensable. Their addition makes the ring OSC circuit have the characteristics of low voltage, low power consumption and high precision at the same time.

4. TEST RESULTS

The chip is manufactured by 0.18 μm CMOS process. When V_{DD} = 0.67V and the temperature is - 40°C -125°C, five chips are tested, and the test results are shown in Table 1. All deviations in Table 1 are calculated based on the situation at 27°C.

It can be seen from Table 1 that the variation deviation of output clock with temperature is within ± 2.5%.

When the temperature is 27 °C, and V_{DD} is 0.6V-0.9V, the test results of five chips are shown in Table 2.

All deviations in Table 2 are calculated based on the power supply voltage V_{DD} = 0.77V. It can be seen from Table 2 that the variation deviation of output clock with power supply voltage is within ± 1%.

Table 1. Variation of output frequency with temperature.

Temperature (°C)	Output frequency value (MHz)				
	#1	#2	#3	#4	#5
-40	1.429	1.54	1.301	1.382	1.312
-20	1.427	1.539	1.309	1.393	1.32
0	1.43	1.535	1.315	1.402	1.329
20	1.442	1.515	1.324	1.412	1.339
27	1.443	1.517	1.328	1.415	1.341
40	1.444	1.519	1.333	1.42	1.346
60	1.436	1.519	1.342	1.426	1.357
85	1.425	1.507	1.348	1.438	1.368
100	1.426	1.499	1.354	1.441	1.371
125	1.441	1.507	1.357	1.443	1.372
Negative deviation (%)	-1.25	-1.19	-2.03	-2.33	-2.16
Positive deviation (%)	0.07	1.52	2.18	1.98	2.31
Total deviation (%)	±1.25	±1.52	±2.18	±2.33	±2.31

Table 2. Variation of output frequency with power supply voltage.

V_{DD} (V)	Output frequency value (MHz)				
	#1	#2	#3	#4	#5
0.6	1.44	1.517	1.334	1.41	1.343
0.63	1.442	1.517	1.333	1.412	1.343
0.67	1.443	1.517	1.328	1.415	1.341
0.7	1.445	1.517	1.325	1.42	1.336
0.74	1.44	1.517	1.324	1.415	1.333
0.77	1.44	1.517	1.322	1.415	1.331
0.8	1.44	1.518	1.32	1.414	1.331
0.85	1.435	1.52	1.317	1.409	1.329
0.9	1.434	1.522	1.315	1.406	1.328
Negative deviation (%)	-0.42	0	-0.53	-0.64	-0.23
Positive deviation (%)	0.35	0.33	0.91	0.35	0.9
Total deviation (%)	±0.42	±0.33	±0.53	±0.64	±0.9

5. CONCLUSION

The ring ICO circuit structure proposed in this study greatly improves the temperature characteristics and power supply characteristics on the basis of the traditional ring VCO circuit through the cooperation of the counter, the bootstrap switch

with special timing control and the special ICO circuit module, so as to obtain a high-precision output clock in the application environment of low supply voltage, and the power consumption of the module is very low. Through testing, the performance of the chip was also verified, and when the voltage was 0.77V and the output frequency was 1.32MHz, the output clock changed with temperature to within ±2.5%, and with the voltage change was within ±1%, and the power consumption was only 382nw.

REFERENCES

[1] Ravezzi, L., "Failure in ring oscillators with capacitive load," *IEEE Transactions on Circuits and Systems I,* 68(8), 3388-3396(2021).

[2] García, A. and Robein, M., "Optimal control applied to TEG harvesting: The necessity of a ring oscillator," *International Journal of Energy Research,* 45(9), 14062-14070(2021).

[3] Osman, H. and Sanchez-Sinencio, E., "A PVT-resilient, highly-linear fifth-order ring-oscillator-based filter," *IEEE Transactions on Circuits and Systems I,* 67(12), 4295-4308(2020).

[4] Shirin, A. and Mohsen, S., "Digitally-controlled ring oscillator for wide tuning range applications," *Radioelectronics and Communications Systems,* 63, 55-65(2020).

[5] Mondal, A. J., Talukdar, J. and Bhattacharyya, B. K., "Variation aware design of controlled voltage swing ring oscillator," *International Journal of Electronics,* 107(1), 99-124(2020).

[6] Mondal, A. J., Talukdar, J. and Bhattacharyya, B. K., "Estimation of frequency and amplitude of ring oscillator built using current sources," *Ain Shams Engineering Journal,* 11(3), 677-686(2020).

[7] Shor, J. and Vinshtok-Melnik, N., "Ultra miniature 1850 μm^2 ring oscillator based temperature sensor," *IEEE Access,* 8, 91415-91423(2020).

[8] Gui, X., Tang, R., Zhang, Y., et al., "A voltage-controlled ring oscillator with VCO-gain variation compensation," *IEEE Microwave and Wireless Components Letters,* 30(3), 288-291(2020).

[9] Choi, M., Jang, T., Bang, S., et al., "A 110 nW resistive frequency locked on-chip oscillator with 34.3 ppm/◦C temperature stability for system-on-chip designs," *IEEE Journal of Solid-State Circuits,* 2016-2118(2016).