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## *High Performance Visible and SWIR Space Camera Heads for Space Applications (3DCM800 & 3DCM830)*



# High Performance Visible and SWIR Space Camera Heads for Space Applications (3DCM800 & 3DCM830)

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## ABSTRACT

3D PLUS has developed in the framework of its R&D activities two new high performance camera heads for space applications. The Centre National d'Etudes Spatiales (CNES) is leading the development of these two new cameras: a 12Mpx space camera head (3DCM800), and a 1.3 Mpx Short Waves InfraRed (SWIR) space camera head (3DCM830). Those camera heads have been integrated using 3D PLUS packaging technology and expertise in order to be as compact as possible and provide the high performances of two images sensors associated with a high performance FPGA based electronic architecture to its Space Camera Product line. Particular attention has been paid to ensure radiation and harsh environment tolerance in order to cover a wide range of application, including equipment or key events monitoring, in-flight spacecraft navigation and rendezvous applications, as well as observation and scientific applications benefiting of the high performance of the sensors (earth observation, hyper/multispectral imaging, planetology).

**Keywords:** Camera, CMOS, SWIR, image sensor, miniaturization, high reliability, space applications

## 1. INTRODUCTION

Following the successful development of its previous Space Camera Head (the 3DCM734, a 4Mpixels CMOS camera head for space applications)<sup>1</sup>, the need to widen the range of applications of such camera heads, by reaching for higher performances, on both the opto-electronic (less noise, higher frame rate, wider spectral bandwidth), and the architectural (improved in-situ processing power and memory) aspects, pushed 3D PLUS to develop new high performances and high resolution camera head for space applications. This was achieved with two new developments : a 12MPx Space Camera Head (3DCM800) offering high optoelectronics performances and readout speed for visible wavelengths, and a 1.3Mpx SWIR Space Camera Head (3DCM830) offering a solution for SWIR targeting applications.

### 1.1 3D PLUS camera heads heritage

From the Rosetta mission with multiple camera heads integrated in Filae's CIVA instrument<sup>2</sup>, to Curiosity's ChemCam Mast Unit instrument integrating a similar camera head in its Remote Micro Imager<sup>3</sup>, 3D PLUS has a long history of providing its packaging expertise for custom integrated camera heads for scientific mission. In the same way 3D PLUS is developing the 3DCM800 and 3DCM830, its previous 4MPx Space Camera Head (3DCM734) was the result of R&D activities with the CNES in order to use its packaging and electronic expertise designing highly integrated electronic modules targeting highly constrained environments, especially for space applications, to create a generic product line of space camera heads. The 3DCM734, as show on Figure 1, is the first generic purpose off-the-shelf camera head for space applications: a 4Mpx camera head, integrating all necessary electronics components to provide an easy-to-use all-in-one solution for space application ranging from simple payload or equipment monitoring, to spectrometry, planetology, or star tracking.

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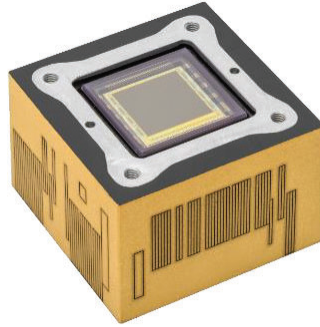


Figure 1. Image of 3D PLUS 3DCM734 Space Camera Head

The 3DCM734 space camera head (3DCM739 for its RGB version) benefits from space heritage, as it successfully took part on the Mars2020 mission in the Remote MicroImager of the SuperCam instrument, mounted on NASA's Perseverance martian rover, taking images of the potential targets of SuperCam's laser, as well as long distance imaging of the planet's surface<sup>4</sup>, as depicted in Figure 2. It is also used as the main camera onboard the EyeSat Nanosatellite.

The 3DCM734 space camera head has also been selected for multiple projects such as the Martian Moon Exploration mission (MMX) as navigation and monitoring cameras as well as the internal Raman spectrometer of the mission rover, Spex One spectro-polarimeter (PACE mission), or Mars Sample Return's Earth Return Orbiter as part of a multi camera monitoring system.

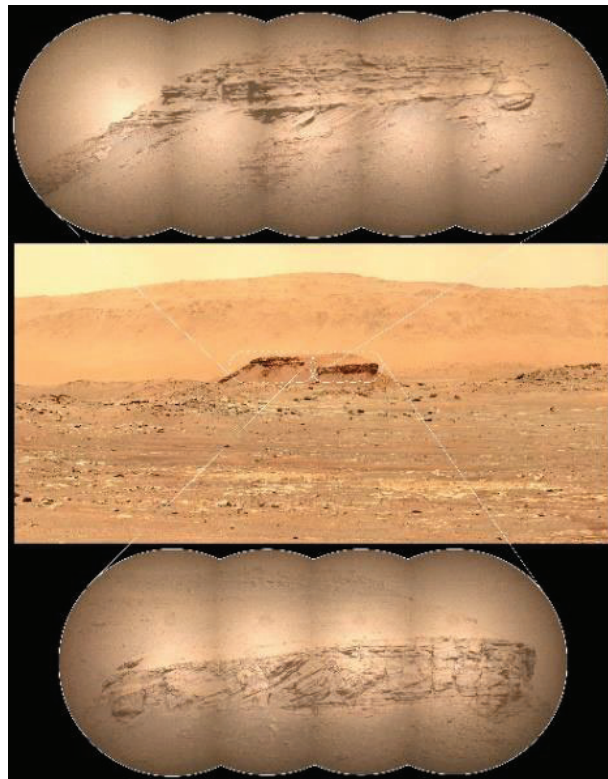


Figure 2. SuperCam Remote Micro-Imager in 'Telescope' mode using the 3DCM734 Space Camera Head – Mesa South of Delta – Sol 63 of the Perseverance Mission. Credit : NASA/JPL-Caltech/LANL/CNES/IRAP

## 1.2 3DCM800 and 3DCM830 Space Camera Heads: Two New High Performance Space Camera Heads Developments

Strong from these multiple successes, 3D PLUS has developed two new high performance camera heads for space applications. With multiple interests in miniaturized camera heads for space applications for future missions of the 2020 decade, the development of the 3DCM800 and 3DCM830 space camera heads aims for a global improvement of the 3DCM734 performances in both opto-electronic and processing power. This improvement takes place at the sensor level on one hand, with increased optoelectronic performances in both the visible and the short-wave infrared wavelengths, and at the electronic level, with an increase of the processing capabilities of the integrated electronic architecture used to control the sensor and interface it with the user system, in order to offer increased image processing capabilities as well as an increased framerate.

## 2. 3DCM800 AND 3DCM830 ARCHITECTURE AND PERFORMANCE

Both camera heads are designed around the association of an image sensor with a high performance Field Programmable Gate Array (FPGA) based architecture. All necessary electronics components for such an architecture, such as memories – for configuration, processing and storage purposes – or power supplies elements – for all active components – are integrated using 3D PLUS integration technology in an highly miniaturized all-in-one 3D cube with reduced volume and mass.

### 2.1 3DCM800 : 12 Mpx Visible CMOS Image Sensor

The 3DCM800 space camera head uses a 12Mpixels global shutter CMOS image sensor integrating on-chip digital image processing and offering a digital interface. The sensor is a Type 1.1inch optical format, and is composed of a 4096 by 3000 pixels matrix. Each pixel is 3.45 $\mu$ m. The sensor offers a digital interface and integrates a digital image-processing unit, allowing for functions such as ROI (Region of Interest) extraction mode, multiple exposure mode, external trigger, multi-resolution pixel readout, to be performed at the sensor level.

### 2.2 3DCM830 : 1.3 Mpx SWIR InGaAs Image Sensor

The 3DCM830 SWIR space camera head uses a 1.3 Mpixels global shutter image sensor with InGaAs focal plane array integrating on-chip digital image processing and also offering a digital interface. The sensor is a Type 1/2 optical format, and is composed of a 1296 by 1032 pixels matrix. Each pixel is 5 $\mu$ m. The sensor offers a similar digital interface as the 3DCM800 12MPx image sensor.

### 2.3 FPGA Based Architecture and Camera Head Design

Both camera head are designed using a similar electronic architecture, as shown in figure 3, to allow a maximized reuse of qualified electronics functions and components as well as software development for the camera heads' FPGA and the electronic ground support equipment.

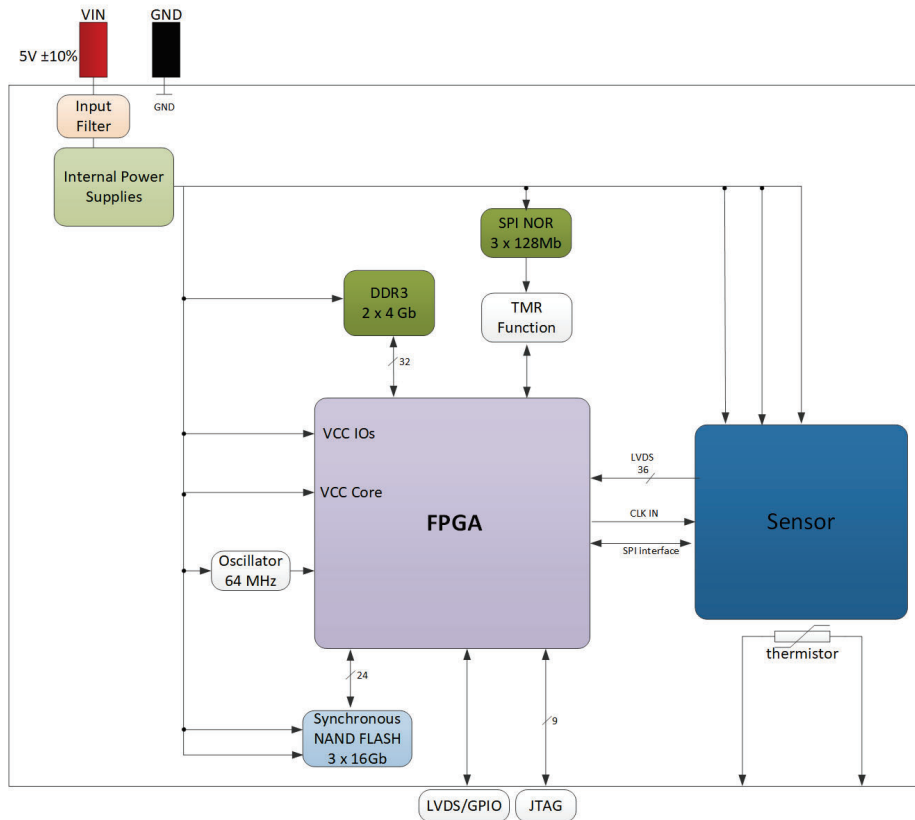


Figure 3. Functional architecture of the 3DCM800 and 3DCM830 Space Camera Heads, detailing its main internal components.

The FPGA core embedded in the camera heads is a high-end SRAM-based FPGA (Kintex Ultrascale). It has a 500 K System Logic Cells capacity, as well as DDR3 interfaces capabilities. The FPGA is directly interfaced with the image sensor, and able to use its associated 8 Gbits of DDR3 volatile memory and 48 Gbits of synchronous NAND Flash non-volatile memories to store data, perform image processing such as compression, correction, or more specific processing depending on its configuration, on the images captured by the sensor, and transmit them or the result of its processing to the system the camera is linked to.

The architecture also integrates a 128 Mbits SPI NOR Flash configuration memory, using a Triple Modular Redundancy (TMR) topology for single event effects (SEE) mitigation, necessary for power-up configuration of the SRAM-based FPGA and for bitstream storage purpose, as shown in figure 4. Three memory components are used a majority voting is performed on read data in order to guarantee the design bitstream integrity when powering up the Space Camera Heads, which is critical for future missions. Each memory outputs (SO0 to SO2), upstream of the majority voting of the TMR implementation, is also connected to user I/Os of the FPGA to allow scrubbing of the memory to either correct or flag bitstream files errors to the user. Moreover, a power switch is also implemented, controlled by the FPGA, allowing the user to switch off the memory components and increase their TID performance by reducing duty cycle, thus increasing their lifetime radiative environments.

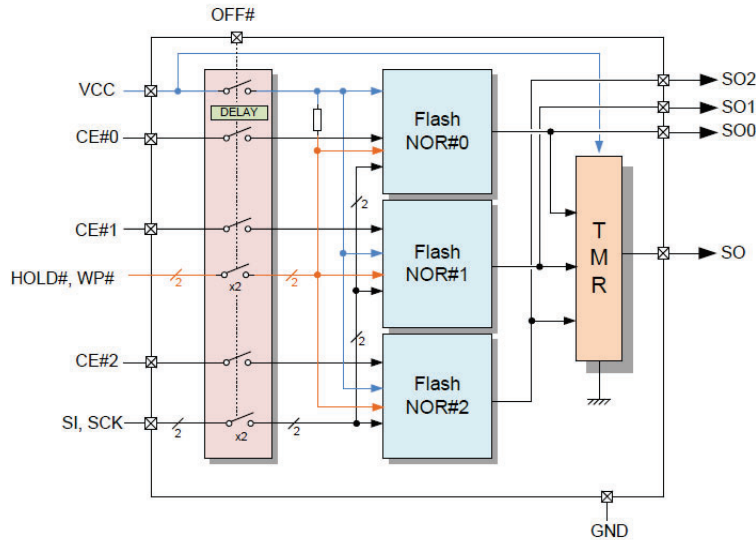


Figure 4. Triple Modular Redundancy implementation of configuration memory for the 3DCM800 and 3DCM830 Space Camera Heads

All necessary power supplies are internally generated by specifically designed Point-of-Load (PoL) converters from the sole 4,5 to 5,5V power input of the camera heads, simplifying their integration in an equipment. The architecture includes an input filter to ensure a good current rejection from the PoL converters to the main supply at the switching frequency. In addition, this ensure the internal PoL converters of the camera heads are protected from high frequency perturbation from the main supply.

For thermal control and monitoring, both camera heads embed two PT1000 thermistors located on the image sensor package and on the copper thermal drain attached to the FPGA bare die. This allow a thermal monitoring of the camera heads when switched off, as these thermistors are accessible through the camera heads PGA pinout. Digital thermal sensor are also accessible via registers monitoring in the image sensor and in the FPGA.

Both camera heads share a 77 Pin Grid Array (PGA) interface, able to cover a wide range of communications interfaces, from SpaceWire to Camera Link ( up to Camera Link FULL configuration), and offering 22 differential pairs, designed for the use of LVDS standard, fully configurable, as well as JTAG interface for firmware loading to the internal configuration memories and FPGA, as well as the power supply interface. The use of a PGA electrical interface also allows for the use of Flex-rigid PCB with multiple compatible space qualified connectors, for easier integration in space equipment.

## 2.4 Camera performances

The performances of the 3DCM800 and 3DCM830 Space Camera Head are described in Table 1 below.

Table 1. Performances of the 3DCM800 and 3DCM830 Space Camera Heads

Parameter	Value	
	3DCM800	3DCM830
Detector Resolution (pixels)	4096 x 3000	1296 x 1032
Pixel Size (µm)	3.45 µm	5µm
Read Noise (electrons)	2 e-	200 e-

Full Well Capacity (electrons)	11 ke-	140 ke-
Dark Current (electrons/s)	< 15 e-/s	< 12 ke-/s
Spectral Response (nm)	400 - 1000	400 – 1800
Quantum Efficiency	71% at 530 nm	75% at 1200 nm
Maximum Framerate	68/64/46 fps in 8/10/12 bit per pixel mode (full frame)	134/125/71 in 8/10/12 bit per pixel mode (full frame)
Volume	40x40x30 mm <sup>3</sup> (+9mm for thermal drain to the module height)	40x40x35 mm <sup>3</sup> ( + 9mm for thermal drain to the module height)
Mass	< 125 g	< 135 g
Input Voltage	4.5 to 5.5 V	
Nominal Power	5W at 25°C (depends of the FPGA configuration)	
Operating Temperature	-40°C to 70°C (opto-electronic performances are temperature dependent)	

## 2.5 Radiation tolerance

In order to answer the needs for space applications and provide a radiation hardened camera head solution in the same manner it was done with the 3DCM734 Space Camera Head<sup>5</sup>, all components used in the 3DCM800 and 3DCM830 Space Camera Heads architecture are selected for their performances regarding radiative environment. The 3DCM800 and 3DCM830 aim to offer radiation performances for SEL immunity up to 62,5 Mev.cm<sup>2</sup>/mg and TID performance above 40 krad (Si).

Irradiation tests have been performed at component level, especially regarding the image sensor performances<sup>6</sup>, which as been deemed acceptable for integration. Further tests are being performed on the 3DCM830 SWIR image sensor, and system level irradiation testing are planned on the camera heads themselves to validate this aspect.

## 3. TECHNOLOGICAL ASPECTS

### 3.1 3D PLUS Stacking technology

Camera head modules are designed and manufactured with 3D PLUS stacking technology<sup>7</sup>. This 3D technology is based on the stacking of electronic components (chips, plastic packages, sensors) reported on a thin PCB, called “flex PCB”. This solution allows testing and screening of each PCB layer before stacking. This is the key feature for building multiple level stacks, while maintaining an acceptable yield. The flex are then stacked vertically and connected together using specific vertical interconnection techniques.

The System-In-Package (SiP) technology allows a gain for the final components regarding weight and volume of a factor 10. It allows combinations that cannot be realized with monolithic System-on-Chip (SoC) approach. This capability domain, referenced as 3D PLUS “FLOW 2”, is qualified by the European Space Agency for Space applications.

This Technology is used for each of 3D PLUS Space Camera heads, including the 3DCM800 and 3DCM830.



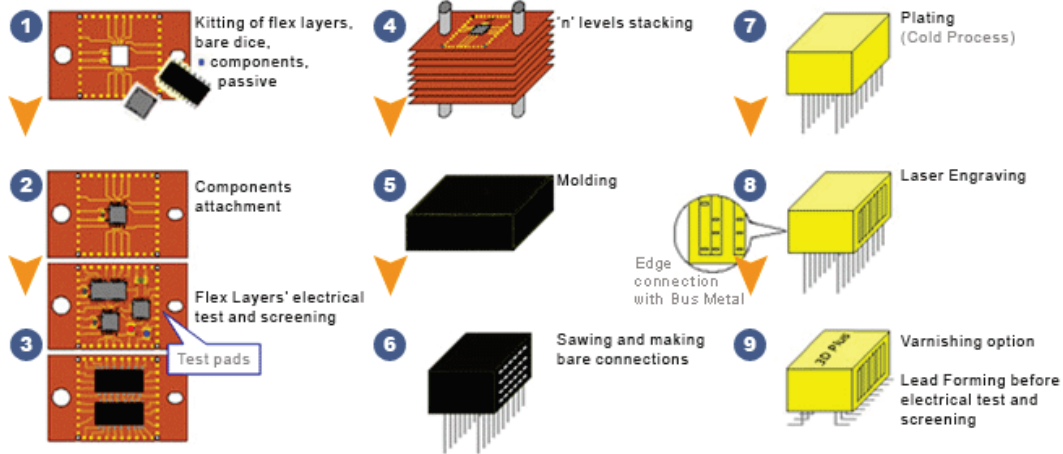


Figure 5. Triple Modular Redundancy implementation of configuration memory for the 3DCM800 and 3DCM830 Space Camera Heads

### 3.2 3DCM800 and 3DCM830 3D Packaging

Taking into account the 3DCM734 previous experience, the integration process for the 3DCM800 and 3DCM830 Space Camera Heads has been improved to allow the integration of the high performances components (Image sensors, FPGA Core) being parts of its architecture as well as dealing with the drawback that accompany them. These drawback for such high performance components are especially the high level of integration needed (small pitch BGA/LGA packages with high number of pins) unusual for design targeting space applications, and the thermal dissipation.

The camera head architecture is divided, based on 3D PLUS technology, in four stacked electronics levels. The top level contains the image sensor, embedded in a metallic cradle, taking the role of optical, mechanical, and thermal interface for the camera head (following the 3DCM734 philosophy, as presented in <sup>1</sup>). The second level contains non-volatile memory components. The third level contain the FPGA core and its processing DDR3 SDRAM memories. The fourth level contain all internal power supplies component. A fifth level is finally used to provide the 77 pins PGA pinout of the resulting cube. The internal organization of the 3DCM800 is described Figure 6.

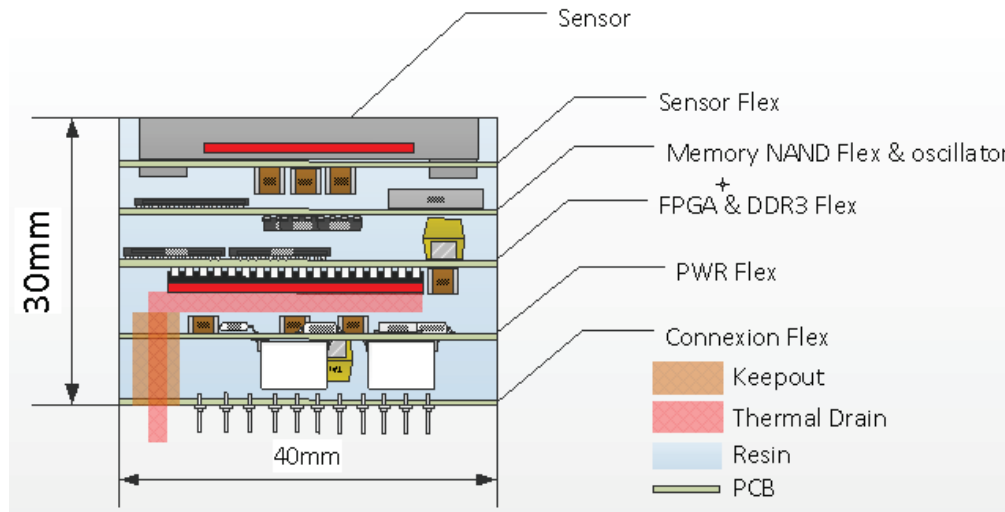


Figure 6. 3DCM800 Space Camera Head Internal Flex PCB stacking



### 3.3 Power Dissipation

The consequent improvement of the electronic architecture processing power used to operate the sensor affected the global need for power dissipation of the module. Compared to the 2W power consumption of the 3DCM734 at 70°C, the 3DCM800 and 3DCM830 power consumption, depending on its configuration and usage, can increase up to 9-10W at 70°C.

As image sensor performances are dependent on the temperature regulation (dark current, readout noise,...) especially for the SWIR detector, and optical equipment rely on temperature stability to keep their precision, the solution chosen in the 3DCM734 Space Camera Head to offer as sole thermal interface the metallic cradle of the sensor was not deemed sufficient in these new developments. The chosen solution for the 3DCM800 and 3DCM830 Space Camera Heads was to double the number of thermal interface and to divide the power dissipation in two areas.

In addition to the metallic cradle solution for the optical/mechanical interface of the camera heads, a new thermal interface has been integrated in the module design to dissipate the power of the most critical hot spot: the FPGA die, and the internal power supplies, which amount for more than 75% of the power consumption of the module. This thermal interface consist in an internal copper thermal drain offering a thermal conductivity higher than the resin used in the 3D PLUS integration process (1 W.m-1.K-1 for the epoxy resin, and 397 W.m-1.K-1 for copper). This drain is placed in contact with the FPGA die substrate (bare-die package) and above the hot spots of the Power flex of the module. It is intended to be connected to a thermal well for dissipating purpose. The Figure 7 shows the internal disposition of the different components as well as the the two resulting thermal interfaces.

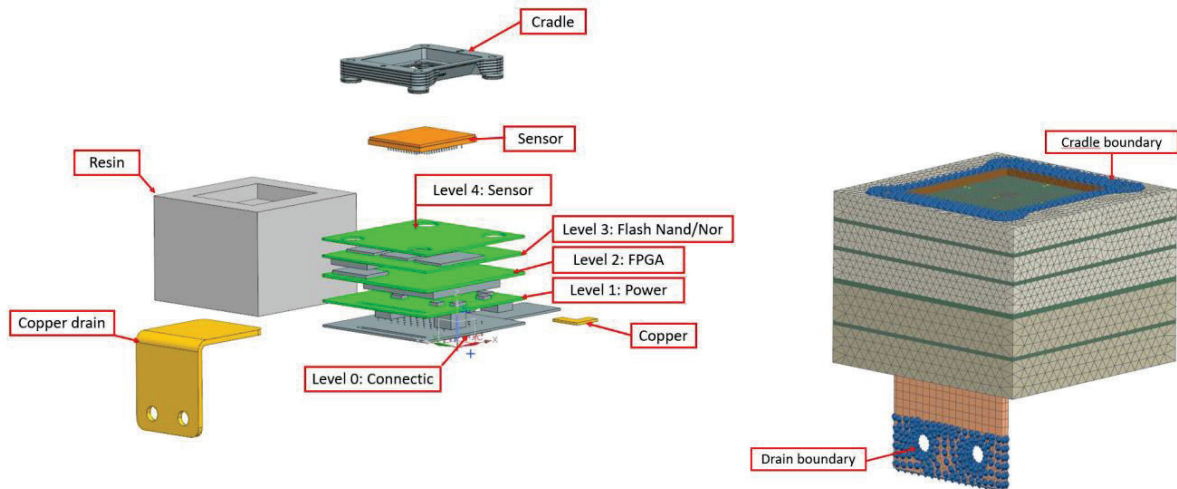


Figure 7. (Left) Internal View of the 3DCM800 Space Camera Head. (Right) Thermal Interfaces of the 3DCM800 Space Camera Head.

Simulations have been performed to theoretically validate the thermal drain integration efficiency and have shown encouraging results.

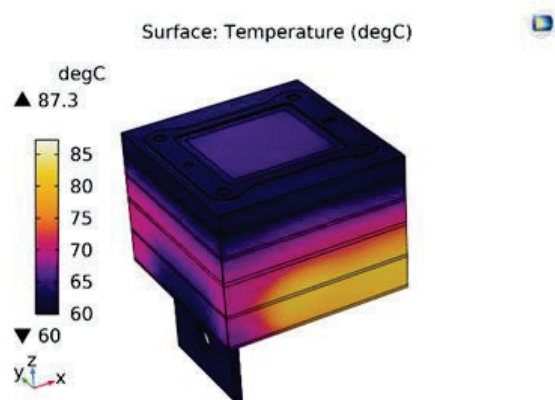


Figure 8. Thermal simulation of the camera head with both thermal interfaces (sensor cradle and thermal drain) connected to temperature well at 60°C.

Initial results of the simulations have shown on average thermal resistance between the cradle and sensor of 3-4°C/W for both camera heads for a maximum power dissipation of 1.5W for the sensors (worst case). This small thermal resistance value allows for a close temperature control of the sensors. In the case of the 3DCM830 SWIR camera head, the cradle was redesigned to increase the thermal interface with the sensor. Indeed, the SWIR sensor used in the camera head sees a reduced contact surface usable to thermally connect the cradle and the sensor. This new cradle design allows a direct connection to the bottom of the sensor package and make the cradle solution as efficient as for the 3DCM800 camera head.

For both camera head, thermal resistances between the thermal drain (bottom) and the FPGA were estimated at 4°C/W, and between the thermal drain and the FPGA Core Voltage converter at 40°C/W.

## 4. MANUFACTURING AND TESTS

### 4.1 Prototypes Testing

Both 3DCM800 and 3DCM830 designs have been successfully tested and validated using 2D demonstrating board, fully representative (components functions) of the final design. These 2D breadboard campaign instigated the reflexion on thermal interface optimization due to FPGA power dissipation.

The 3DCM800 3D prototypes were manufactured and successfully tested and characterized over the full operational temperature range, validating the expected performances. The figure 9 show the power consumption of one representative prototype at -55°C, 25°C and 70°C in three different state : FPGA not configured, FPGA configured and camera configured in IDLE mode, FPGA configured with camera in continuous image capture mode (25fps full frame).

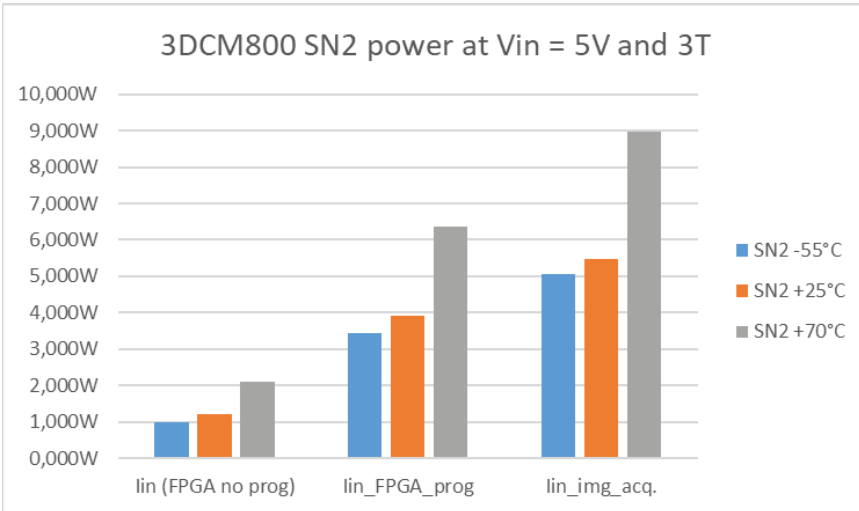


Figure 9. Power consumption at -55°C, 25°C, and 70°C.

Figure 10 shows the distribution of power consumption of three different 3DCM800 camera head prototypes.

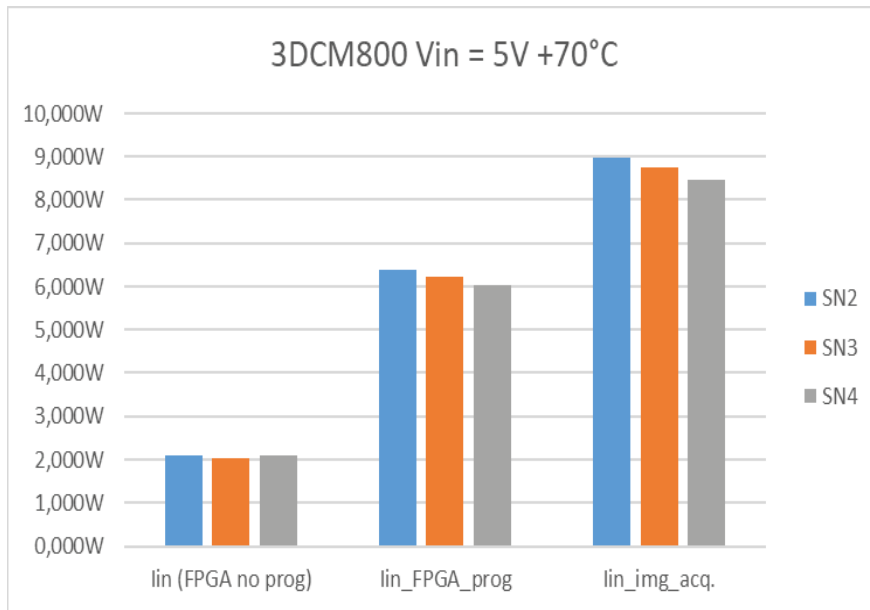


Figure 10. Power consumption distribution at 70°C (3 samples).

Thermal aspects have been considered and TVAC tests have been performed on the 3DCM800 prototypes to validate thermal simulations. Those tests are still ongoing and being analyzed when this paper is being written.

Prototypes picture of the 3DCM800 are shown in Figure 11.

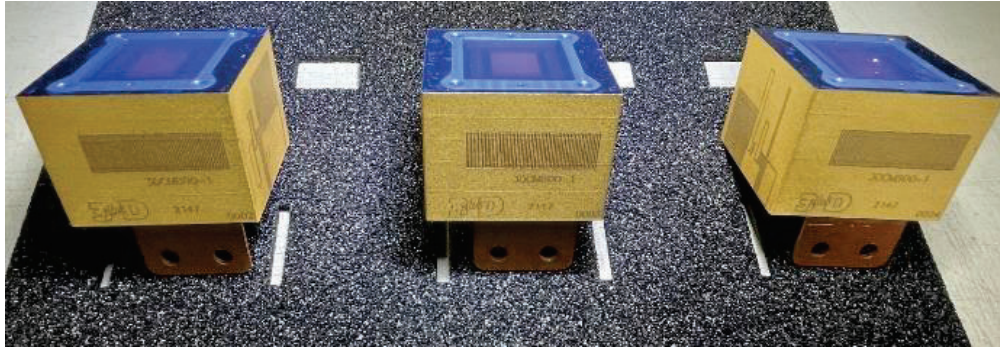


Figure 11. Functional Prototypes of 3DCM800 Space Camera Head

#### 4.2 Future Tests and qualifications to be performed

3DCM800 camera heads prototype flight models are being manufactured and shall be submitted to qualification testing including thermal cycling, HAST, life test. Available prototypes will continue TVAC testing and will be submitted to mechanical testing (vibrations and shock) and EMC testing at module level.

3DCM830 SWIR camera heads first prototypes are being submitted to initial characterization and testing in the next few months before following the same qualification testing performed on the 3DCM800 camera head.

### 5. CONCLUSION

In the framework of its R&D activities, and to answer the need of future space mission to provide a high-performance and high-resolution space camera head, 3D PLUS developed two new Space Camera Head, thus improving the performances and capabilities of its existing camera products. These developments have required new technological solutions to ensure the full range of functionality in highly constrained environment regarding radiation effects, and temperature. The 3DCM800 and 3DCM830 Space Camera Head are expected to answer the needs of future space mission for a wide range of applications. The improvements of performances will especially allow to address applications for which advanced opto-electronic and processing performances are required.

3DCM800 and 3DCM830 Engineering Grade Modules have already been manufactured and tested (under tests for the 3DCM830) and are already available for order. Qualification of both space camera heads are planned to be completed in 2023.

### 6. ACKNOWLEDGEMENTS

The authors wish to thank the Detection Chain team at CNES for their support in these new developments, allowing 3D PLUS to develop the 3DCM800 12Mpixels and 3DCM830 SWIR Space Camera Heads for future space missions.

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