Future Trends in Electronic Packaging

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ABSTRACT

Electronic packaging is traditionally defined as the back-end process that transforms bare integrated circuits (IC) into functional products. As the IC feature size decreases and the size of silicon wafer increases, the cost per IC is reduced and the performance is enhanced. The future IC chips will be larger in size, have more input/output terminals (I/Os), and require higher power. In addition to the advancements in IC technology, electronic packaging is also driven by the market requirements for low cost, small size, and multi-functional electronic products. In response to these requirements, packaging related areas such as design, packaging architectures, materials, processes, and manufacturing equipment are all changing rapidly. Wafer-level packaging (WLP) offers the benefits of low cost and smallest size for single chip packages, since the package is done at wafer level other than individual die. After packages reach the horizontal limit of dimensions, 3D stacking solution provides more efficient packages through expanding packages in the vertical dimension. Functional integration is achieved with 3D stacking architectures. System in package (SiP), one of the solutions to system integration, incorporates electronics, non-electronic devices such as optical devices, biological devices, micro-electro-mechanical systems (MEMS), etc, and interconnection in a single package, to form smart structures or microsystems. MEMS devices require specialized packaging to serve new market applications. This paper and presentation describe the technology requirements and challenges of these advancing packaging areas. The potential solutions and future trends are presented.

Keywords: Electronic packaging, interconnects, MEMS, smart structures, wafer-level packaging, 3D packaging, system-in-package

1. INTRODUCTION

Following the famous Moore's Law over thirty years, the number of transistors in a single integrated circuit (IC) chip doubles every 18 to 24 months. However, packaging of these ICs is far behind this scaling and has been a limit factor in cost and performance of electronic products for years. Electronic packaging serves important functions such as protection, powering, and cooling chips and components to provide electrical and mechanical connections between these parts and the outside world. The input/output (I/O) connection pads on the integrated circuit are connected to corresponding terminal pads on the package using wire bonds or solder bumps with flip chip technology.

As chip pin counts increase in an integrated circuit to include not only the transistor(s) but additional crucial components of an electronic system for higher performance and increasing functionality, the interconnection becomes a complex process addressing electrical noise and electromagnetic interference with close signal proximity, thermal issues with high current and a proper thermal management and heat dissipation without sacrificing coupling efficiency, and mechanical issues with miniaturized structures. The problem becomes more complex when electronic packaging involves medical implantable devices addressing needs of the human body to regulate, monitor, sense, detect, deliver medical doses, or enhance bodily functions to enable remote diagnostics and patient independence to enhance the quality of human life. Micro- and nanoscale packaging is critical for device interconnection and system integration involving various technical challenges due to the complexity of device functions and operating environment.

To meet these challenges, the electronic packaging technology has evolved from a simple metal can and soldered metal wiring to complex multilayer ceramic and organic structures depending on the applications (medical applications, automotive electronics, optoelectronics, military, and consumer) with provision of proper hermeticity and improved electrical and thermal performance. Embedded or integral passive components are embedded within the substrate layers producing three dimensional packages with minimum volume and efficient electrical and thermal performance. Via holes between the layers can provide electrical connections and good thermal management. Usually, the various substrate

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layers carrying interconnections, bare devices, and passives are laminated under heat and pressure and then heat treated to produce a compact structure. Finer features for low cost ceramic packaging are attained with well developed photoimageable material formulations.

Micro-electro-mechanical systems (MEMS) such as bio-MEMS, RF-MEMS, optical MEMS and inertia MEMS require specialized packaging to serve the diverse applications. For instance, bio-MEMS are MEMS designed for medical and/or biological applications where these devices are built on a single silicon wafer merging electronic and mechanical functions to sense, control, and move objects on a certain scale. Like ICs, the MEMS devices need to be packaged to provide a contact to the user. Packaging requirements such as small size, light weight, low production cost, high operating frequency with good electrical performance, high reliability, good yield, and high reaction rate are necessary to produce efficient systems with minimum invasion to the environment.

Demands for multifunction, small size and low cost in modern consumer electronic markets require packaging that combines wireless and mixed signal devices, optoelectronics, and MEMS chips. New packaging types such as wafer-level packaging, 3D packaging and system-in-package are evolving in response to these demands.

2. SINGLE CHIP PACKAGING

The Semiconductor Industry Association (SIA) recently released the 2005 International Technology Roadmap for Semiconductors (ITRS). This roadmap projects the semiconductor technology in near-term years (2005 - 2013) and long term years (2014 - 2020) [1]. The roadmap projections can be used as a guideline to develop novel packaging technologies to meet the requirements of future ICs.

Figure 1 illustrates the single-chip packages technology requirements of low cost and high performance products in terms of cost per pin, chip size, maximum power, I/O count, and performance. These two categories of products are selected since they represent the extreme cost and performance requirements of future ICs, respectively. Low cost products such as consumer electronics, hand-held, memories, disks, displays, etc, have a strong cost constraint, while high performance products like work stations, avionics, and supercomputers require the highest performance. Packages must provide cost and performance solutions to all these products.

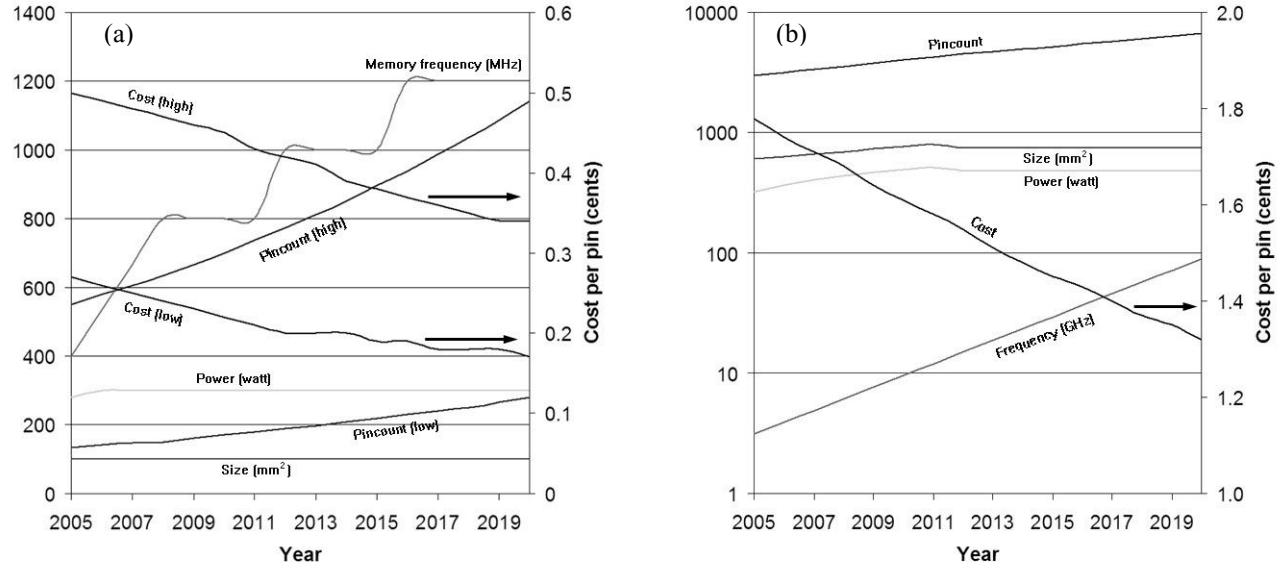


Figure 1: Single-chip packages technology requirements for (a) low cost (b) high performance products. (Data source: ITRS [1])

Today, the package costs as much as the die or even more in some cases. The packaging does not have the same Moore's law scaling advantage as ICs have, to improve performance and reduce cost simultaneously. Therefore, the decrease in packaging cost is much slower than in IC cost. The high packaging cost is a result of the increased IC performance such

as larger dice, higher I/O counts, higher power level, and higher frequency. In addition, the R & D work in packaging technologies is not aligned with the rapidly changing IC technologies. To cut packaging cost down, new design methodologies, innovations of technologies, materials, and equipment must continue to come.

The largest chips today are on the order of is 26 mm x 23 mm. As the process yield improves, the chip size will likely increase to be 30 mm x 25 mm in five years. The number of I/Os will increase from 3180 in year 2006 to 6600 by year 2020. The maximum power needed in 2006 is 365 watts, but this will be as high as 480 watts in 2020. As for the frequency, six years later, the packages for high performance products need to operate at 14.9 GHz, while those packages for memories must work properly at 1 GHz. Currently, these frequencies are 3.9 GHz and 667 MHz, respectively.

As can be seen in Fig. 1, the chip size, I/O counts and power needs are usually associated with one another. Larger die and finer feature size create more I/Os, and higher power must be provided to these large dice. The increase in power needs poses challenges in thermal management. In addition to the increased signal I/Os, higher operating frequency and higher power density also necessitate more I/O pins in packages for the power and ground, to keep the signal integrity.

High I/O counts place the largest challenge to packaging interconnects. Wire bond pitch will decrease to 30 microns in 2008. Afterwards, there will be a demand for 25 micron and under. However, the manufacturable solutions do not exist. The decreasing flip chip area array pitch provides a solution to the increasing number of I/Os and power density. The flip chip bump pitch will shrink from today's 130 μm to 110 μm in year 2008. Technologies for less than 100 μm pitch flip chip need to be developed.

Package substrates contribute to the majority of package cost and are also the performance limiting factor. High density interconnect substrates use micro vias and finer traces to meet the interconnect challenge. Figure 2 illustrates 50 μm diameter micro vias fabricated in high density low temperature cofired ceramic substrates. In addition to the added cost, the improvement in interconnect density leads to more crosstalk between parallel signal lines since these lines are closer. Several areas such as material properties need to be improved to meet the ITRS cost and performance projections.

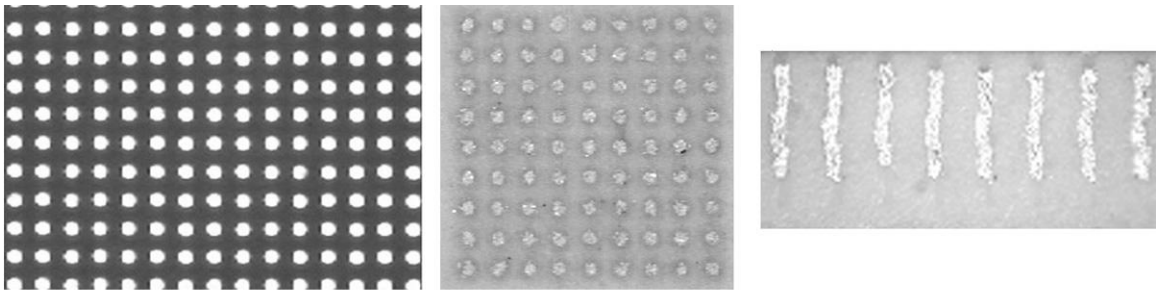


Figure 2: Photograph of 50 μm diameter micro vias for multilayer low temperature cofired ceramic substrates.
(a) punched vias (b) vias filled with silver conductor paste (c) cross section of fired vias (Not to scale)

3. WAFER-LEVEL PACKAGING

Wafer-level packaging (WLP) is a technology to package ICs at the wafer level before singulation. In traditional electronic packages, ICs are diced, tested and then packaged in packaging foundries. WLP merges the back-end packaging into the front-end wafer fabrication. Packaging, testing, and burn-in are all performed at wafer level immediately after the wafer fabrication.

Wafer-level packaging has been driving by the demand for very low cost and chip size packages from portable and hand-held electronics markets. WLP reduces the packaging cost by up to 70% compared to chip scale packages (CSP) and ball gird array (BGA) packages. The factors contributing to the cost reduction include packaging, testing, and burn-in as well as the reduced space required on the printed circuit boards (PCB). Since the I/O redistribution and package interconnects

are done on the wafer, no additional package is needed. In addition, the larger the wafer size, the lower packaging cost per device, as more devices are packaged using almost the same process. At least 50% of the cost can be reduced from testing and burn-in at the wafer level, instead of individual die. Furthermore, since the area array flip chip interconnects yield truly chip size packages, only a chip size area is needed on the PCB board for the package-to-board assembly. As a result, tremendous space saving on the PCB board is achieved, compared to quad flat packages (QFP) and wire bonded chip-on-board (COB) with the same die size.

Currently, WLP is mainly used to package small dice (< 10 mm) with low I/O counts (< 100). No under fill is needed when assembling these small packages. Cell phones are the largest beneficiary of this technology. WLP is also extended to the packaging of optical devices and MEMS, which will be discussed in-depth in a later section.

While producing significant benefits, packaging at the wafer level possesses inherent disadvantages as well. Bad dice are packaged along with the good ones, and bad packages may occur on top of good dice. Testing several hundreds of devices on a 300 mm diameter wafer simultaneously at a full power level presents challenges to the test fixture, such as the large force applied to the test fixture, huge power and heat dissipation, and coefficient of thermal expansion (CTE) mismatch between the test fixture and the silicon wafer. As the I/O counts per die go up, under fill is necessary to ensure the reliability of package assembly, and the pitch of PCB bonding pads may not match the fine pitch of solder bumps on the package.

The development of WLP technology is proceeding in the following areas: higher I/O counts, larger dice, integration of passive components (resistors, capacitors, inductors, filters, and transmission lines) in the redistribution layers, wafer-level 3D packages, and new applications.

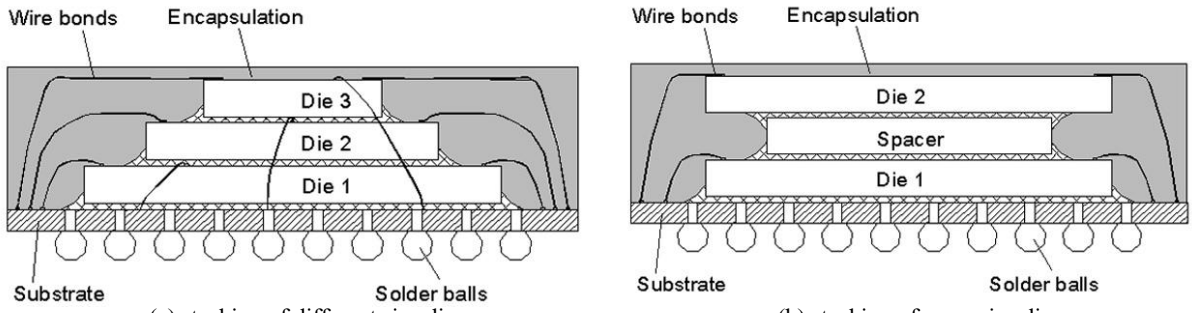
4. 3D STACKED PACKAGING

The market trends are toward smaller, lighter, and more functional cell phones and compact electronics. Since chip scale packages and wafer-level packaging technologies have reached the chip size- the horizontal dimensional limit of packages, a natural next step for more volume efficient packages is to take advantage of the vertical dimension. This is the goal of 3D stacked packaging. Compared to the system on chip (SOC) solution, 3D stacked packaging offers significant advantages in package and system cost, time-to-market, form factor, performance, and design flexibility [2], as it eliminates the difficulty in integrating different types of devices onto single silicon chip and the long global interconnect across a large die.

Although various designs and processes have been explored for 3D packaging, stacked die and stacked package are the two commonly accepted strategies. Die stacking provides low package profile and low package cost due to the least substrate consumption. The drawback includes the need of known good die (KGD) and single-source product. To solve the KGD issue, a pre-tested package (usually CSPs) can be staked in or on top of another package, resulting in a package on package or package in package stacking. In addition, packages from different suppliers can be stacked, which offers the flexibility of device selection.

In a typical wafer-level 3D stacked-die packaging process, separate wafers with small die size are fabricated, followed by wafer bonding, thinning, inter-die interconnection, and molding encapsulation. By stacking two or more ICs with different functions, 3D packaging creates a functional integration. For example, most cell phones now have the stacked die packages for flash, SRAM, and/or memory(s) stacked on logic. In addition, 3D packaging has found its way into memory cards, PDAs, Bluetooth, and more products. Currently, 3D packages in high-volume production stack two to four dice with low I/O counts, small die size, and modest power needs. Packages with more than five dice are currently under development.

Different size bare dice are typically stacked in a format of pyramid as shown in Fig. 2(a), while a blank silicon chip or an elastomer spacer is placed between the same or similar size dice to form an overhang for inter-die interconnection (see Fig. 2 (b)). Dice with a thickness of 100 μm are used in production, and thinner dice are in development. The overhang of 1.3 mm is common. With regard to the inter-die interconnection, wire bonding is the most popular technique due to its low cost, while other methods such as a combination of wire bonding and flip chip as well as through-wafer vias are also utilized, depending on the application requirements.



(a) stacking of different size dice (b) stacking of same size dice

Figure 2: Typical 3D stacked die packages.

Stacked die packaging is driving the development in several areas: low loop wire bonding, wafer thinning, through-wafer vias, and thin molding. The complexity of 3D stacked configuration and the limited space between the stacked thin dice pose challenges for the wire bonding. The loop height of the lower tier must be minimized to avoid the shorting the wires between different tiers. The top tier wires must have low loop heights as well to keep the wires inside the molding materials and achieve a thin package. The standoff stitch bonding (SSB) technique addresses the low loop requirement. In contrast to the conventional ball bonding, the SSB bonds the ball on the substrate first, and then the stitch on the gold bump previously formed on the die pads. Loops lower than 100 μm are achieved. For ultra-thin packages, gold wedge bonding and ultra-low loop bonding can produce bonding loops under 75 μm and longer wire spans. In addition, when bonding to overhangs, die edge bouncing may cause problems such as die cracking, loop damage, and inconsistent bumps. Therefore, the bonding parameters must be carefully optimized.

To achieve thin packages or allow more dice to be stacked in a package without increasing the package height, the wafers must be thinned from the original thickness of 300-500 μm down to 100 μm or under. This is done by a combination of backgrinding and etching. A typical wafer thinning process begins with a coarse grinding to remove the bulk of the wafer thickness from the backside of device wafer, leaving a 15-20 μm thick grinding damage layer into the bulk silicon. A fine grinding then removes most of the mechanically damaged layer. The last 15-30 μm materials are etched away using a wet etchant $HNO_3/HF/H_3PO_4$ or plasma, to produce smoother surface and remove the layers containing defects or micro cracks. Wafers with thickness of 75 μm (300 mm diameter) are in production, and the projected wafer thickness in 2010 is 50 μm. Since wafers thinner than 100 μm are very fragile, the device wafer must be mounted on a wafer carrier at the device side prior to the thinning process, if the desired final wafer thickness is less than 100 μm.

Through-wafer vias significantly reduce the average wire length of block-to-block interconnects by providing shorter vertical interconnection instead of spreading them out horizontally. At high operating frequencies, through-wafer vias interconnection provides the best performance due to the lowest parasitic capacitance and inductance of interconnects. The "Bosch Process" is a widely used process to create through-wafer via interconnection. This process uses alternating etch (SF_6) and deposition (C_4F_8) cycles to produce high aspect ratio through-wafer vias that have extremely straight sidewalls. Next, an insulation layer e.g. SiO_2 is formed on the sidewalls, followed by the deposition of an adhesion/barrier layer (TiN) and copper seed layer. Electroplating fills the through-wafer vias with copper. Lastly, a chemical mechanical planarization (CMP) technique is performed for the planarization of Cu electroplated vias. Through-wafer vias from 4 to 20 μm in diameter with 25 to 50 μm via pitch have been demonstrated by a number of researchers.

3D stacked packaging will be a choice technology for future interconnect-limited devices. However, it also presents challenges as previously mentioned and concerns regarding heat removal, package yield, wafer to wafer alignment, and final test. As this technology expands to more applications, much research work needs to be conducted to address these issues.

5. SYSTEM-IN-PACKAGE (SiP)

SiP incorporates devices such as integrated circuits, passive components, non-electronic devices e.g. MEMS, and interconnection substrate to form a complete system or subsystem in a single package. SiP enables the integration of different functions such as sensing, communication, and data processing. SiP is driven by the consumer electronics with the requirements of increasing functionality and reducing cost as well as size. As an alternative to the system-on-chip approach, SiP offers faster time-to-market, lower development cost, and greater flexibility [3].

Several technologies are available for the implementation of SiP at substrate and wafer level. The substrates for SiP include ceramic, silicon, glass, and laminate. The interconnection between semiconductor devices and the substrate is accomplished using wire bonding and/or flip chip techniques. The passive components are mounted to the substrate through surface mount technology, or embedded in a multilayer substrate using techniques such as low temperature cofired ceramic, thin film, or organic laminate. The 3D stacking architectures can also be used in the SiP. Moreover, SiP has the capability to embed simple thin dice into the build-up layers of organic substrates, leaving the surface area for the high value devices.

The key issue in SiP is the incorporation of different types of device and component involving various technologies and materials. Known good die and test are the major challenges in the realization of SiP. Design tools for system integration are required as well.

The future SiP will integrate nano-scale devices into micro-scale and macro-systems. The key is to couple the nano-structures to large-scale platforms. Combination of biological and non-biological components is critical for systems for bio- and medical applications.

6. PACKAGING OF MEMS DEVICES

6.1. MEMS and applications

MEMS are functional microdevices integrating mechanical elements, sensors, actuators, and/or communication electronics on a common substrate or in a package. The mechanical or electromechanical components in MEMS range in size from micrometers to millimeters, and are fabricated using integrated circuit compatible micromaching process that etches away the sacrificial materials of a silicon wafer or adds new structural layers onto the wafer. MEMS enable the development of a variety of advanced microsystems to sense and act to the physical and chemical quantity in the environment.

MEMS components and subsystems are widely used today [4]. Millions of pressure sensors are utilized in vehicles for fuel vapor pressure measurement. Accelerometers meet the low cost requirements of airbag systems. Ink-jet printer heads, large screen TVs and micro mirrors for PC projectors are also in mass production. Many more products are in low volume and prototype, such as angular rate sensors, radio frequency (RF) switches, optical networks, biomedical sensors, micropumps, gas sensors, to name a few. The emerging applications include high resolution displays, microfluidics, chemical analysis, medical diagnostics, and drug delivery.

Future applications demand MEMS on the system level that have the MEMS and circuitry together. For example, airbag microsystems incorporating the deployment circuitry can decide whether to inflate the airbags. Another trend is the micromachined sensing systems providing several functions, such as optical and wireless, pressure and temperature, and acceleration and angular rate sensing. With the reduction of feature size down to submicron to nanometer, nanoelectromechanical systems (NEMS) can sense and actuate at the level of molecule for various applications.

6.2. MEMS packaging and challenges

Packaging is a critical aspect of the realization of these applications, as all MEMS devices need to be packaged and the packaging accounts for 70-90% of the product cost. MEMS packaging includes post-processing release, package fabrication, assembly, testing, and reliability assurance. Although many micromachining processes for the fabrication of MEMS devices originate from the mature IC fabrication techniques, the packaging requirements of MEMS devices are more stringent than the requirements of most ICs. In addition to the requirements for ICs such as electrical interconnect, mechanical support and thermal management, the package must also allow the MEMS devices to interact with the

environment while isolating the devices from the environment. Therefore, it is unlikely to apply IC packaging technologies to MEMS devices directly.

MEMS devices present several challenges to the packaging engineers. Due to the diversity of functions and applications of MEMS devices, there is no standard packaging technique for most MEMS devices. The complexity of MEMS requires the package to be co-designed with the MEMS chips. The lack of design standards and modeling tools is an issue. The chip, package and environment must be compatible. For instance, the package materials in biosensors that have contact to biological matter must be biocompatible. Improper packaging design, process, and materials adversely affect the performance and/or reliability of MEMS components. The temperature above 100°C for bonding bio-MEMS components may denature deoxyribonucleic acid (DNA) and most proteins. The thermal stress resulted from the mismatch in coefficient of thermal expansion between the die and the substrate leads to performance degradation and resonant frequency shift. Outgassing can cause stiction of beams or membranes.

6.3. Conventional MEMS packaging

Ceramic package and molded plastic package are commonly used in high volume MEMS products. In both types of packages, the hermetic seal of MEMS devices is critical for many MEMS devices to operate properly. A hermetic seal eliminates moisture on the MEMS surface that may cause stiction of the free-standing MEMS devices, and protects the die from particle contamination as well as chemical contact to the package materials.

Ceramic package provides a hermetic vacuum environment for the MEMS die through a metal lid seal. Molded plastic packages are ideal for low cost and high volume MEMS products, since they tend to be less expensive. However, molded plastic packages are not truly hermetic and are not as reliable as ceramic packages. To protect the die from contact with the molding material and moisture, the MEMS devices need to be capped at the wafer level through a wafer-to-wafer bonding technique. Wafer bonding yields a hermetic seal and is achieved by means of silicon direct bonding, anodic bonding, eutectic bonding, or glass frits bonding. Since the wafer bonding is accomplished before dicing the MEMS devices, it eliminates a lot of processing issues such as handling, stiction of device, and contamination.

Gel coating is another option to protect the die in plastic package [4]. Silicone gel has been used in electronic industry for many years for corrosion protection. Furthermore, the gel does not transfer thermal stress to the die. The gel coating is usually inside a plastic package. However, in some applications such as pressure sensors, the gel is exposed to the environment, so that the MEMS device can interact with the environment. Dispensing gel with high throughput and tight volume control presents challenges.

A ceramic package has a cavity housing a MEMS die. The MEMS die is attached onto the bottom of cavity at the backside through a solder or an epoxy adhesive. Lead frame or laminate substrate in molded plastic package offers a platform for the die attachment. Care must be taken when selecting a solder or an epoxy adhesive as the die attachment material. The MEMS die must withstand the processing temperature for die attachment. Solders produce a strong rigid bonding and the MEMS die may have some extent of thermal stress due to the CTE mismatch and temperature cycling. In the case of epoxy die attachment, such an adhesive must be used that no outgassing will occur, as any deposition of materials on the MEMS surface has influence on its performance.

Gold or aluminum wires connect the MEMS die to the package using the established wire bonding technique. The I/O interconnects of MEMS packages can be peripheral (dual-in-line package or quad flat package) or area array (ball grid array or pin grid array), depending on the number of I/Os needed and application requirements.

6.4. Advanced MEMS packaging

As mentioned previously, the future demand for MEMS is the integrated smart microsystems combining sensing, actuating, optical, and/or electronic functions. Advanced packaging must be pursued to meet this requirement. Integrated monolithic MEMS are one of the options to consider. Since the microstructures and microelectronics are integrated on a single chip, the monolithic MEMS will have reduced size and improved performance. However, the incompatibility of processes for MEMS and the processes for CMOS presents tremendous challenges. In the monolithic MEMS that have been demonstrated, either MEMS or CMOS can be fabricated first.

Instead of putting devices on a single chip, several MEMS sensors with different functions and integrated circuit dice can be assembled onto a common multiple layer substrate that offers interconnect among the dice, resulting in multi-chip module (MCM) MEMS. The interconnects from dice to MCM substrate are achieved using wire bonding or flip chip techniques. Flip chip technique bonds the die top-side-down onto the substrate. The flip chip bumps on the dice have small pitch, can be made in a format of area array, and produces a small gap between the dice and the substrate. As a result, flip chip bonding provides high I/O count, reduced size, and extremely low inductance and capacitance per joint. With flip chip and MCM, a compact complex system can be achieved. The added packaging expense is one of the disadvantages of MCM packaging. In addition, MCM packaging is not suitable for capacitive MEMS sensors, as the bonding pads in the package generate capacitance that will affect the sensing.

Wafer-level packaging technology has also been adapted for MEMS packaging. Since the MEMS devices are encapsulated at wafer level prior to singulation, a number of processing associated issues can be avoided, such as damage to the MEMS components during handling and contamination from wafer dicing. Various WLP solutions to MEMS packaging can be used as long as they are able to provide a hermetic enclosure for the released MEMS devices and to be compatible with MEMS fabrication as well as packaging processes. Among the demonstrated WLP approaches for MEMS, through-wafer via interconnect is a promising technique. In this method, cavities above the MEMS devices and through-wafer vias are fabricated in the capping wafer using a wet etch or deep-silicon reactive ion etch (DRIE) process, depending upon the via size and density. Metallization of the through-wafer vias is then carried out by means of sputtering or electroplating. Copper and gold are two commonly used conductors for the via interconnects. The wafer bonding and via connection to the MEMS wafer are performed simultaneously. This technique is favored due to its space efficiency and low parasitic capacitance and impedance.

6.5. Future trends

Future MEMS packaging will still be application and function specific. A variety of solutions will co-exist. However, much packaging R & D effort in the following areas will be emphasized:

- 3D integrated miscrosystems with ASICs fabricated in the capping wafer that is bonded onto the MEMS wafer at wafer-level packaging.
- Standard packages for each category of functional MEMS products, such as RF, optical, inertia, biomedical, microfluidics, to reduce the packaging cost.
- Standards and CAD tools for packaging that cover mechanical, electrical, microwave, thermal, optical, and chemical functions.
- New and effective assembly tools and methodologies.

CONCLUSIONS

The advancing semiconductor technology and the rapidly changing markets have been driving the new innovations of electronic packaging. While these innovations provide solutions to the ultimate goal of high performance at low cost, they present many challenges in all aspects of the realization of these technologies. In order to meet the packaging challenges, more investment and efficient collaboration in R & D work are required.

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