Cost of Ownership for Soft-X-Ray Projection Lithography*

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ABSTRACT

We present a general analysis of cost of ownership for an integrated circuit production lithography system. We illustrate the method with examples from i-line and deep ultraviolet lithography, as well as soft-x-ray projection lithography. Tool utilization is emphasized as well as system throughput. Our analysis suggests that with 20 wafer per hour throughput, which may be attainable with soft-x-ray projection lithography, lithography costs will rise to four times today's i-line costs, or higher. In addition to throughput, reticles and photoresist will be cost drivers for this technology.

1. INTRODUCTION

Soft-x-ray projection lithography (SXPL) has generated considerable excitement in the integrated circuit (IC) community because it has demonstrated sub-0.1-μm resolution with reduction printing.[1] Thus it holds forth the tantalizing possibility of ultra-large scale integrated circuit (ULSI) fabrication with resolution of that order. This is a task that cannot be accomplished with either i-line or deep ultraviolet (DUV) lithography.[2] I-line technology is now firmly entrenched in IC manufacturing of 0.5-μm critical dimension (CD) devices. DUV lithography is seen as the most likely usurper for the 0.25-μm CD device generation, yet it is not having an easy time gaining a foothold in manufacturing. The reasons for this are two: One is that the technology is still being put through its paces by the process development community to assess its robustness; the other is that it is not yet clear that it is cheap enough to offer a good return on investment. If SXPL is to be successful it will likewise have to meet stringent technological and cost requirements.

Ceglio and Hawryluk[3] have made a first cut at assessing CoO for SXPL with a model in which different cost and performance parameters were allowed to vary by up to ±30%. In their analysis they identified throughput as the major factor in determining lithography costs. However, they neglected two parameters that significantly affect throughput in a step-and-repeat, or step-and-scan, system: step time, that is the time to move from one field to the next, including any local focus and/or alignment time; and stepper overhead, that is the time required for wafer transport, leveling, and global alignment. For optical steppers in use today, these two times account for roughly two thirds of the total wafer throughput time. While throughput appears to be the dominant factor affecting lithography costs for systems used in production today, and is considered likely to dominate SXPL costs, a review of some of the systems now under evaluation for manufacturing future device generations will show that photoresist or reticles can cost as much as five or ten times today's prices, and in those situations their costs can dominate over throughput.

Another factor that is coupled to throughput and that must be considered to obtain accurate cost figures is tool utilization. In our discussions, the term throughput, when unmodified, means raw throughput, or peak throughput, i.e. the number of wafers per hour that a system can process when it is being fully utilized. But no system is ever fully utilized, and thus average throughput is the product of utilization and peak throughput. Costs rise rapidly as tool usage time drops. Finally, the design of SXPL imaging and condenser systems has continued to evolve, as have estimates of the probable dose and processing requirements for photoresists at soft-x-ray wavelengths. Consequently, we present a new analysis of CoO for SXPL, based on the methods of Arnold,[4] that incorporates these changes.

We are aware that CoO modeling is sometimes viewed with skepticism. Critics say: (1) that the true CoO depends largely on yield, and yield is difficult to predict; (2) that 5 to 10% differences in perceived costs between two pieces of equipment are often based upon inputs that are known with only 20 to 30% certainty, if they are known with any certainty at all; and (3) that the inputs to the CoO model can usually be manipulated so as to produce any outcome that is desired by the modeler, whether that outcome is realistic or not. These are all valid criticisms. Nevertheless, CoO remains a useful exercise.

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The toolmaker who neglects to do this piece of homework can easily fail to sell his product either because he has underestimated his customer's requirements, or he has overlooked a competitor's capabilities, or he has ignored a major flaw in his design. Further, CoO modeling is one of the metrics used by IC manufacturers to compare competing tools prior to procurement.

In this paper we attempt to provide a broad picture for lithography CoO. We do this by presenting a comparison of some i-line steppers. We illustrate the impact of photoresist cost by modeling CoO for DUV lithography. We provide some historical data on capital costs for steppers. We offer some data pertaining to reticle usage, and we explore the effects of reticle usage and cost on CoO. We then model CoO for SXPL by working from best guesses for future equipment prices, projections for x-ray power delivered to the wafer plane, typical overhead times taken from steppers in use today, and likely resist processing costs and requirements. And we point out some issues that are unique to SXPL that may have a negative impact on throughput and tool utilization unless they can be adequately addressed in the system design. We do not claim that our analysis predicts what the true cost of SXPL will be. That would be impossible and it is not our goal. We seek to illustrate the method for computing costs so that those who are working on SXPL can decide for themselves whether or not the technology can be made marketable and how best to go about it.

2. COST OF OWNERSHIP EQUATIONS

In our analysis we make use of five equations. The first of these is for system throughput, which is defined in units of wafers per hour (wph) as

$$T = 3600/(t_{OH} + N\times(t_{STEP} + t_{EXPO})), \tag{1}$$

where N is the number of steps on the wafer and the overhead, step, and exposure times are given in seconds.

The utilization-and-throughput-dependent lithography cost per-wafer-level-exposure (pwle) in dollars is calculated from

$$C_{UTD} = C_{LPH}/(T\times U) \tag{2}$$

where U is the fraction of scheduled production time during which the system is actually in use, and C_{LPH} is the lithography cost per hour, which is given by

$$C_{LPH} = C_{ED} + C_L + C_{FP} + C_M. \tag{3}$$

In Eq. (3), C_{ED} is the capital equipment depreciation cost per hour; C_L is the per hour labor cost of running the lithography system; C_{FP} is the cleanroom cost per hour associated with the system footprint; and C_M is the per hour cost of maintaining the system. The utilization-and-throughput-independent cost pwle is given by

$$C_{UTI} = C_C + C_R \tag{4}$$

where C_C is the pwle cost of consumables, such as photoresist, and C_R is the pwle reticle cost. The total pwle cost is then given by

$$C_{TOT} = C_{UTD} + C_{UTI}. \tag{5}$$

In generating the data plotted here, we made use of the lithography worksheet, which is contained within the SEMATECH CoO spreadsheet calculator.[5] We exploited only a few capabilities of the spreadsheet. For example, we ignored the impact of defect densities and of CD and overlay yield losses on cost, not because they are unimportant, but because equipment that cannot deliver acceptable yield will not sell. In our view, yield is best considered separately from CoO when comparing systems prior to purchase. We did not extend our analysis beyond the lithography worksheet, and thus we do not present any data that takes account of administrative and engineering overhead, non recurring engineering costs, insurance, and the like.

In addition to setting the CD and OL yield to 100%, we modified the reticle cost pwle parameter so that we could vary or hold constant the number of wafer levels exposed per reticle at will. For each of our plots we have specified the number of wafers that was used, either in the input table or directly on the plot.

3. TWO EXAMPLES: i-LINE AND DUV LITHOGRAPHY COO

Table 1. lists the input values that we used for calculating CoO for i-line and DUV steppers that were recently evaluated by our company. In Figs. 1 and 2 we have plotted Eq. 5 for three of the most competitive i-line tools with tool utilization as the ordinate. We assumed that 90% of the wafer would be covered with dice. In Fig. 1 we used the full field for each stepper to arrive at the number of steps required; for Fig. 2 the number of steps was calculated based on the number of dice that would fit in the stepper field.

Table 1. CoO Inputs for i-Line and DUV steppers

Parameter	Value
i-Line Stepper Capital Cost	$2.0-2.9M
DUV Stepper Capital Cost	$4.0M
Stepper Maintenance Cost	$12/hr.
Coat/Develop Track Capital Cost	$1.6M
Track Maintenance Cost	$10/hr.
Equipment Lifetime	5 years
Scheduled Production Hours per Day	24 hrs.
Scheduled Production Days per Year	350 days
i-Line Stepper Footprint	100 ft^2
DUV Stepper Footprint	150 ft^2
Resist Coat/Develop Track Footprint	50 ft^2
Cleanroom Cost	$1.5K/$ft^2$
Reticle Cost	$3.4K
Wafer Levels per Reticle	2400 wlpr
Wafer Size	200 mm
i-Line Resist Cost	$800/gal.
DUV Resist Cost	$8K/gal.
Resist Usage	6 ml/wafer
ARC Cost	$675/gal.
ARC Usage	6 ml/wafer

Table 2. i-Line Variables Affecting Throughput

Parameter	Value
Power to the Wafer Plane	2.0-2.3 Watts
Intensity at Wafer Plane	500-570 mW/cm^2
Field Size	4.0-5.1 cm^2
Die Size	0.8×0.9 cm^2
Dose Requirement	200 mJ/cm^2
Exposure Time (t_{EXPO})	0.35-0.40 sec.
Step Time (t_{STEP})	0.3-0.48 sec.
Steps (full field)	65-71 steps
Steps (dice per field)	66-99 steps
Overhead Time (t_{OH})	24-28 sec.
Throughput (full field used)	41-52 wph
Throughput (based on dice/field)	33-51 wph

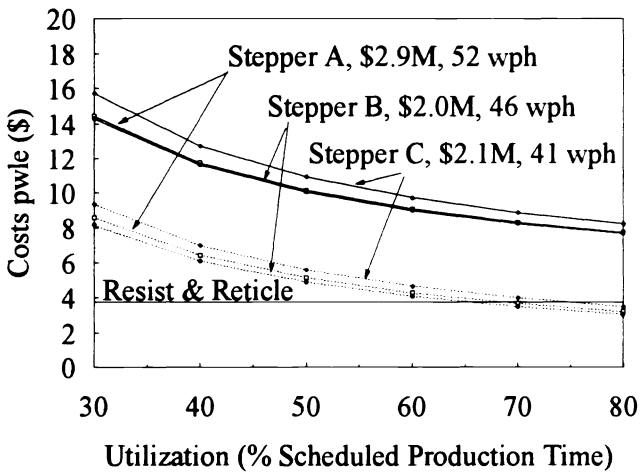

Figure 1. CoO for three i-line steppers. Solid curves include all cost; dotted are capital equipment depreciation only. Full stepper field was used for throughput calculation.

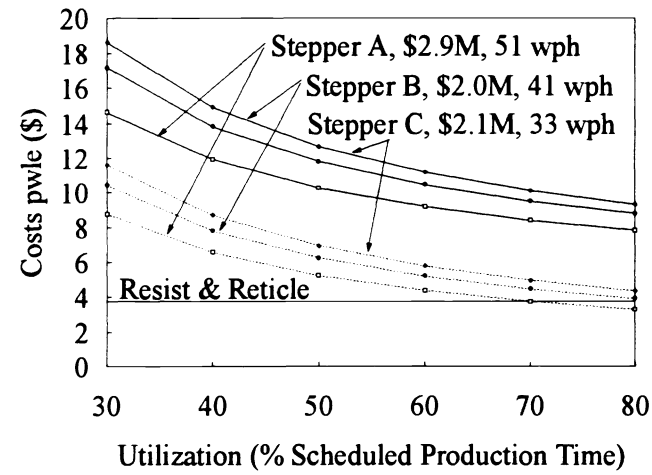

Figure 2. CoO comparison for three i-line steppers where Stepper A can accommodate six dice/field, but B and C have room for only four.

Stepper A has the highest price, but because of its superior throughput, it comes out in the middle when it's capital cost is considered on a pwle basis, as can be seen in Fig. 1. When the entire cost, including the coat/develop track, is included, Steppers A and B are identical in pwle cost. If throughput is calculated on a die/field basis, as in Fig. 2, the throughput for each tool declines. But for the particular example used here, Stepper A's throughput has only changed slightly. And since it can accommodate 6 dice/field as compared to 4 dice/field for either of the other steppers, it is now the most cost-effective of the three. Note that in the 70 to 80% tool utilization range, where IC fabs target operation, the reticle and coating costs represent ~40% of the total cost of $8 to $10 pwle.

In Fig. 3 we plot the pwle cost for a DUV stepper having raw throughput of 60 wph for today's resist price of $8K/gal. and for a projected price of $2K/gal. At $8K/gal, the pwle materials cost for coating exceeds the entire litho pwle cost for i-line, even for tool utilizations as low as 30%. At $2K/gal, the total pwle cost comes closer to being in line with i-line, but DUV is still more expensive. Throughput in Fig. 3 is taken to be 60 wph based on a dose of 20 mJ/cm^2; the real dose that will be required in production may be closer 50 mJ/cm^2.

Plots such as those in Figs. 1 through 3 might be used to decide how many steppers to buy for a fab, assuming a particular utilization can be achieved. What the plots do not tell is what the pwle cost would be if too high a value of utilization is assumed and lithography becomes the fab bottleneck. It is for this reason that preventative maintenance schedules and requirements for calibration and engineering tests are closely evaluated prior to stepper purchase.

Table 3. DUV Variables Affecting Throughput

Parameter	Value
Power to the Wafer Plane	0.16-1.1 Watts
Intensity at Wafer Plane	40-230 mW/cm^2
Field Size	4.0-7.0 cm^2
Dose Requirement	20 mJ/cm^2
Exposure Time (t_{EXPO})	0.09-0.70 sec.
Step Time (t_{STEP})	0.3-0.55 sec.
Steps (based on full field)	41-71 steps
Overhead Time (t_{OH})	24-53 sec.
Throughput (using full field)	30-75 wph

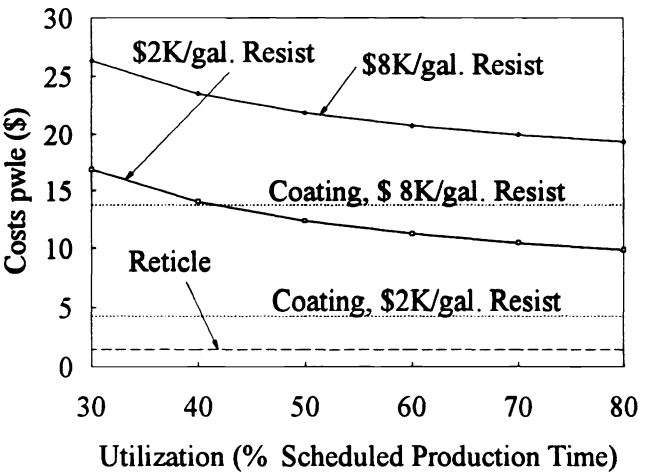

Figure 3. CoO for DUV lithography for today's cost of $8K/gal. resist, and for projected resist cost of $2K/gal resist.

4. IMPACT OF RETICLE COST AND USAGE

For purposes of considering reticle usage, semiconductor chips can be divided into two broad categories: high volume products such as memories; and low volume products such as application specific integrated circuits (ASICs). It is believed that ASICs account for about 10% of the IC market, and that these are evenly split between semicustom designs that require only 2 to 4 custom reticles and custom designs that require a complete reticle set.[6] Further, it is estimated that at least 50% of ASICs do not meet design specifications and must be reworked. One might anticipate that reticle cost would have an impact on this market. But the assumption is sometimes made that most reticles in fabs other than ASIC facilities are used to process a great many wafers. While it may be true that there a few tens of factories worldwide that generally produce large wafer volumes per reticle set, these are likely to account for only a small percentage of the total number of reticles used by the semiconductor industry. And even high volume products typically go through repeated process modifications and device shrinkages.

In Fig. 4 is plotted the combined output of two of our company's fabs in terms of wafers out per device for a single year. There are 136 devices plotted in all. Some of these are static memories, others are logic devices. In Fig. 5 the devices have been grouped according to the number of wafers produced for each where the wafer quantities have been rounded up to the nearest 100. The average number of wafers per device is ~2400. But, for most devices a smaller number of wafers is produced; the median quantity is 570. We can only draw inferences from the data because what is not readily available is how many of the devices have low volumes because the product is being ramped up or down, how many devices have multiple reticle sets associated with them, how many revisions were required to obtain the final mask set, and how many reticle sets were needed simply to develop the technology. The primary inference to be drawn is that the real cost attributable to reticles is higher than is commonly assumed.

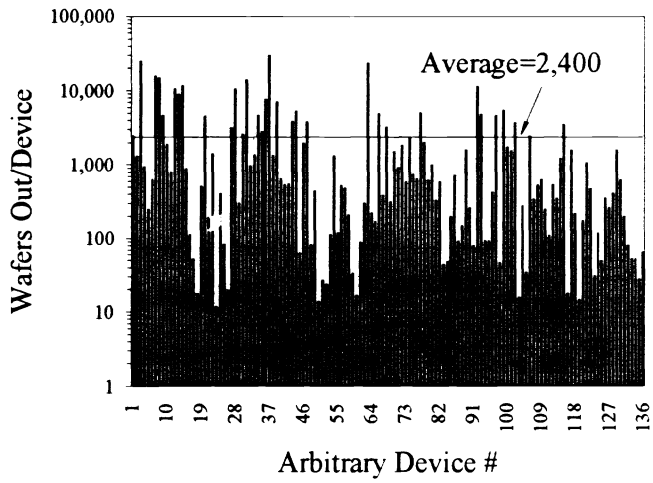

Figure 4. Histogram of wafers out per device can be taken as an indication of reticle usage.

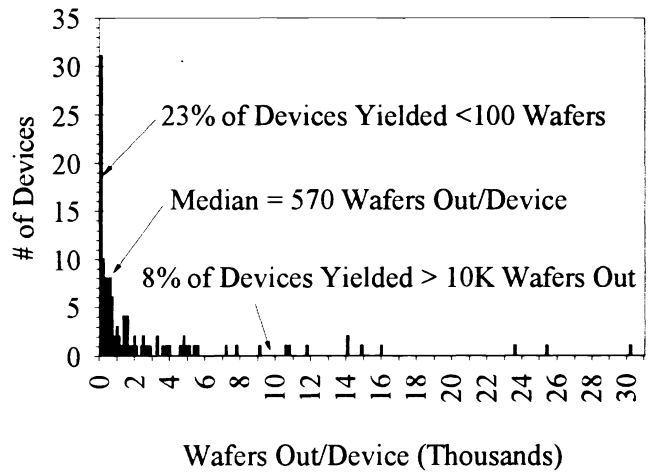

Figure 5. Devices are sorted according to the number of wafers produced in a single year per device. Wafer quantities are rounded up to the nearest 100.

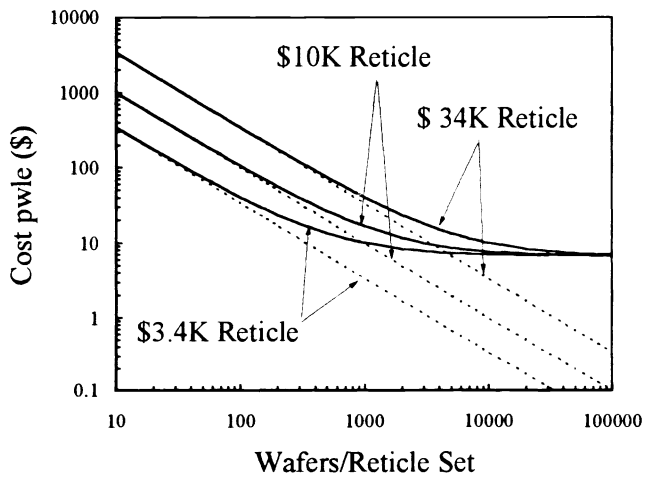

Figure 6a. Lithography costs pwle for i-line as a function of the number of wafers process per reticle set for today's reticle prices and assuming 3× and 10× cost increase. Dotted lines are for reticle cost per wafer alone.

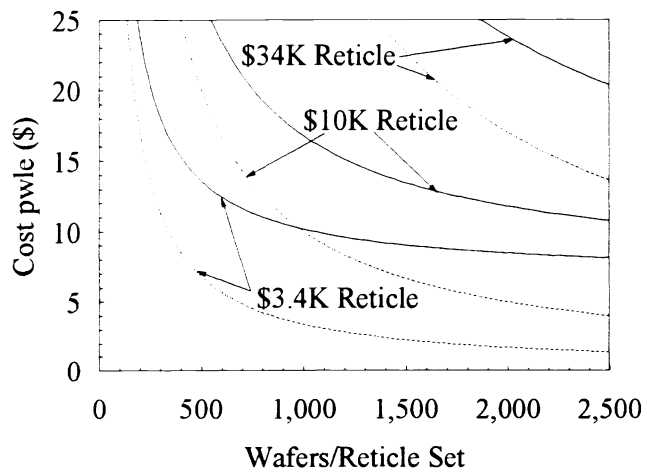

Figure 6b. The same data as in Fig. 6a but plotted on a linear scale.

In Fig. 6a and 6b we consider the effect of reticle cost for an i-line system with 50 wph throughput and 75% tool utilization. We have included plots for an average reticle price of $3.4K, and for possible phase-shift mask prices. At today's prices, for wafer quantities of under 100, the lithography system comes for free as compared to the reticle cost. From Fig. 6b we can see that for quantities of 500 wafers, the pwle cost has increased ~20% due to the reticle as compared with a 2500 wafer volume. For a volume of 2400 wafers processed per reticle set, the cost of the reticle at $3.4K, $10K, and $34K represents 17, 38, and 68% of the total litho pwle costs, respectively.

5. STEPPER COST AND THROUGHPUT

In Fig. 7 we illustrate the cost, in unadjusted dollars, of steppers that were purchased by our company within the past 15 years. If this trend continues, the cost of a stepper purchased in the year 2000 will be $8.2M.

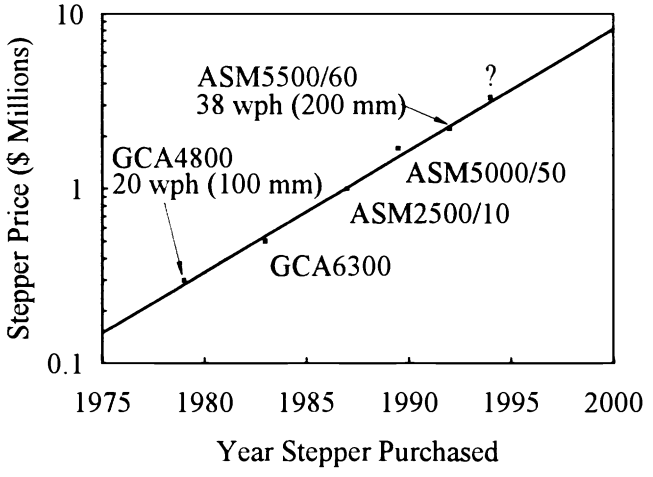

Figure 7. Stepper cost as a function of time. The data points indicate actual purchase price. The curve is a least squares fit of the data.

6. SXPL COST OF OWNERSHIP

In Tables 4 through 7 we have listed our assumptions for SXPL CoO modeling. Many of these numbers are best guesses, but some warrant special mention because in our estimation it will take considerable engineering effort to achieve them. For example, the stepper overhead time of 30 seconds is approximately the same number as for i-line steppers today. Yet unlike i-line, SXPL has to contend with a vacuum environment, which necessitates electrostatic wafer chucking[7] and wafer travel through a load-lock system with associated pumpdown times. Without careful planning, this time could rise by a factor of 2 or more.

We have assumed a silylated resist scheme[8] because of the short absorption length in virtually all materials at λ=13 NM.[9] This is only illustrative; other schemes have been proposed.[10] Throughput of a single silylation unit is ~20 wph; thus if 60 wph throughput was desired, three units would be need to operate in parallel.[11] We have also added in the cost of a pattern-transfer etch station. Such a system might likewise require three chambers to compensate for low throughput.

The dose that will be required for SXPL has been estimated to be in the range of 1 to 10 mJ/cm^2.[12] However, more recently that estimate has been adjusted upward.[13] It is worth noting that no resist other than PMMA, which requires 55 mJ/cm^2, has demonstrated 0.1-μm resolution at λ=13 NM.[1] In this analysis the maximum dose that we consider is 20 mJ/cm^2 because at that dose throughput has dropped to ~ 20 wph, which is slower than most IC manufacturers would be willing to consider for a production tool, and most researchers are confident that a 20 mJ/cm^2 goal can be met. The assumptions for losses in the

condenser and imaging systems, given in Table 6, are based on the ongoing work of Sweatt[14] and will need to be adjusted as research proceeds.[15] Although we used a laser plasma system in our analysis, a synchrotron based design might equally have been chosen for examination.[16] For that system, the quantity of interest, power delivered to the wafer plane, is roughly comparable with that delivered by the system reviewed here.[17]

Table 4. SXPL Cost of Ownership Inputs

Parameter	Value
Stepper Capital Cost	$7M
Stepper Maintenance Cost	$12/hr.
Resist Coat/Silylate Track Capital Cost	$1.6M
Track Maintenance Cost	$10/hr.
Track Throughput	60 wph
Equipment Lifetime	5 years
Scheduled Production Hours per Day	24 hrs.
Scheduled Production Days per Year	350 days
Stepper Footprint	150 ft^2
Resist Coat/Silylate Track Footprint	50 ft^2
Cleanroom Cost	$1.5K/$ft^2$
Reticle Cost	$10K
Wafer Levels per Reticle	2400 wlpr
Wafer Size	200 mm
Resist Cost	$2K/gal.
Resist Usage	6 ml/wafer
Resist Pattern Transfer Etcher Cost	$2M
Etcher Maintenance	$10/hr.
Etcher Footprint	50 ft^2
Etcher Throughput	60 wph

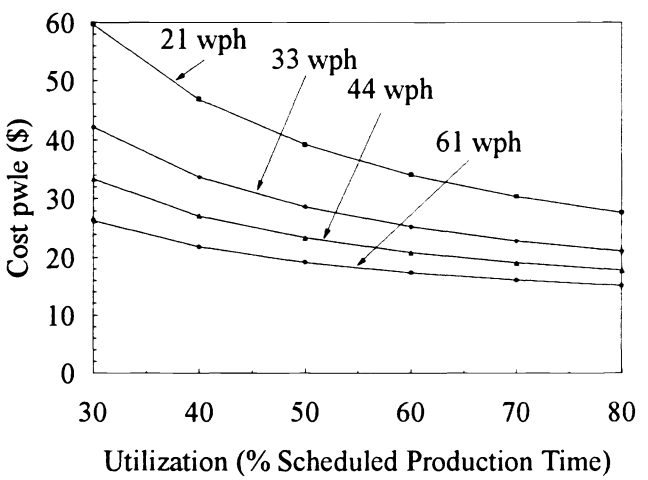

Figure 8. CoO for SXPL system with 60 mW to wafer plane. The numbers of 21, 33, 44, and 61 wph correspond to doses 20, 10, 5, and 1 mJ/cm^2, respectively.

Table 5. SXPL Stepper Cost Breakdown

Parameter	Value
Source: Laser	$0.8-1.5M
Synchrotron/Beamline	$1.6-2.0M
Condenser/Imaging System	$1.5-2.0M
House, Alignment, Step & Scan	$4.0-5.0M

Table 6. X-Ray Power Transmitted to Wafer Plane

Parameter		Value
Laser Power		500 Watts
X-Ray Conversion Efficiency		1.5%
Photons Collected		50%
Condenser Mirrors:	(2) @ 10°	0.88 (ea.)
	(1) @ 15°	0.80
	(1) @ 25°	0.71
	(1) ~⊥, MLC	0.68
Imaging Mirrors:	(3) MLC	0.68 (ea.)
Reticle:	(1) MLC	0.68
Si Windows:	(2) 200 NM thk.	0.70 (ea.)
Bandwidth Narrowing: $(4.5)^{-1/2}$		0.47
Realism Factor		1-0.5
X-Ray Power to Wafer Plane		30-60 mW

Table 7. SXPL Throughput Variables

Parameter	Value
Power to the Wafer Plane	30-60 mW
Scan Intensity at Wafer Plane	12-24 mW/cm
Field Size	2.5×variable cm^2
% of t_{EXPO} Spent on Overscan	20%
Dose Requirement	10 mJ/cm^2
Scan Speed	1.2-2.4 cm/sec.
Exposure Time (t_{EXPO})	1.25-2.5 sec.
Scan Time (t_{STEP})	0.5 sec.
Steps (2.5×2.5 cm^2 field)	46 steps
Overhead Time (t_{OH})	30 sec.
Throughput (full field)	21-33 wph

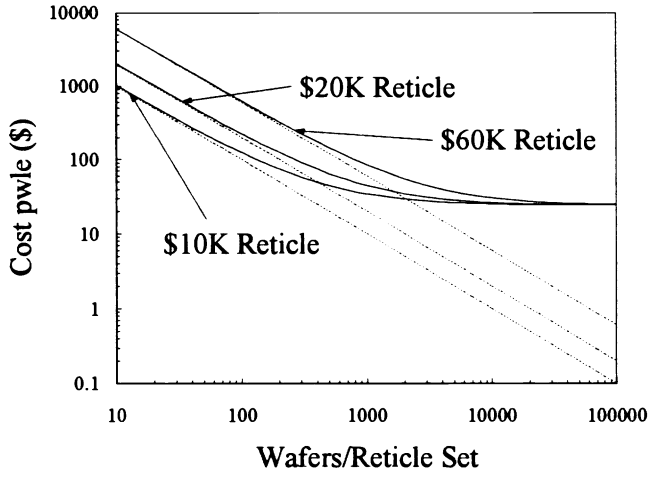

Figure 9. Impact of reticle cost and usage on SXPL CoO.

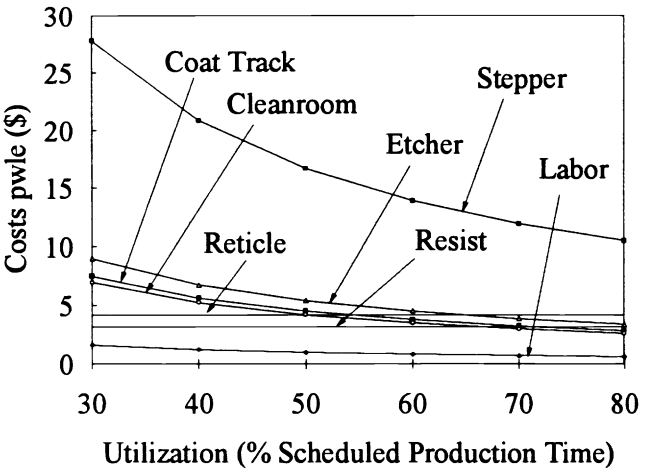

Figure 10. Cost breakdown for SXPL for 20 wph throughput.

The input value for normal incidence multilayer reflectivity of 0.68 per mirror is higher than values that are typically obtained today. A "realism factor" can be used to account for deviations from the 0.68 value, as well as for any other losses within the system. Losses can be caused by slight mismatches in mirror bandpasses and can occur at apertures. In analyzing power delivered to the wafer plane, we have ignored the impact of wavefront distortion caused by optics heating.[18,19] Further analysis of substrate materials and system designs is needed. It is conceivable that mirror heating will be the factor that ultimately limits the deliverable x-ray power.[20]

In Fig. 8 we plot lithography costs pwle for SXPL for doses varying from 1 to 20 mJ/cm^2 with the assumption of 60 mW power delivered to the wafer plane. At 75% utilization and 1 mJ/cm^2, the pwle cost is ~ $17 pwle, almost 2× higher than for i-line today. At 20 mJ/cm^2, the cost rises to $32 pwle.

In Fig. 9, we consider the impact of reticles that cost $10K, $20K, and $60K for a system with 20 wph throughput. Assuming 2400 wafers processed per reticle set, the reticle cost represent 15, 25, and 50%, respectively, of the total pwle cost. From the breakdown into components of the SXPL pwle cost in Fig. 10, it can be seen that, for the inputs from Table 4, the dominant cost driver is the stepper. However, a higher reticle price or better stepper throughput could alter this picture.

7. SCHEDULED DOWNTIME

A factor that will adversely impact tool utilization is the need to periodically remove built-up carbon deposits from the Mo/Si multilayer mirror surfaces.[21,22] The mirror contamination is caused by the interaction of the x radiation with gaseous residuals in the vacuum system, as well as with species that outgas from the photoresist as it is being exposed.

The deposits can be removed by in-situ dc oxygen discharge cleaning,[21] or by ultraviolet ozone cleaning.[22] The required cleaning time is estimated to be ~ 30 minutes, but the acceptable mean time between cleans is not yet known.[23] Added to the cleaning time will be the time required to recalibrate the x-ray flux. This could be done through running a test wafer, but that would be time consuming. Far preferable would be an accurate, rapid, in-situ calibration system.

8. CONCLUSIONS

We have illustrated a method whereby CoO for a lithography system can be computed. We presented examples from i-line and DUV lithography, as well as SXPL. We emphasize the inclusion of tool utilization as well as raw throughput. Our analysis indicates that reticle cost and usage has a much larger impact on pwle costs than is widely assumed, and that sharply increased

reticle cost, whether for phase-shift masks, x-ray proximity printing, or SXPL reflective masks, will have a dramatic impact on overall lithography costs. We also show that for DUV lithography the pwle cost is dominated by the comparatively high cost of photoresist, although this picture will change if resist prices drop.

Our analysis of SXPL, which is based on what we believe is the best information available today, indicates that the pwle cost is likely to be 4 to 5× higher than today's i-line pwle costs of ~$8 pwle. In arriving at this tentative conclusion we made a number of assumptions that we view as optimistic, such as assumptions about power to the wafer plane and stepper overhead time. Perhaps with innovative engineering and design these assumptions can be met, or even proved conservative.

Can these increased costs be supported for future device generations? If we are to hold to the SIA roadmap that targets complete silicon processing costs at ~$4 cm^2,[24] the likely answer is no. A twenty mask process at $30 pwle would consume 50% of the $4 budget. A question yet to be answered is whether or not tomorrow's IC market can support higher prices.

Finally, we stress this is not the definitive word on CoO for SXPL. What we have presented is a working model that can and should be modified as analysis of the various technical aspects SXPL system design evolve.

9. ACKNOWLEDGMENTS

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10. REFERENCES

1. O. R. Wood II, J. E. Bjorkholm, J. Bokor, L. Eichner, R. R. Freeman, T. E. Jewell, W. M. Mansfield, A. A. MacDowell, L. H. Szeto, D. M. Tennant, W. K. Waskiewicz, D. L. White, and D. L. Windt, "High-resolution soft-x-ray projection imaging," in Soft-X-Ray Projection Lithography, Vol. 12 of OSA Technical Digest Series (Optical Society of America, Washington, D.C., 1991), 40-42.
2. D. W. Johnson and C. A. Mack, "Modeling the continuing realm of optical lithography," Semiconductor.International 15, 134-140 (1992).
3. N. M. Ceglio and A. M. Hawryluk, "Wafer cost analysis for a soft-x-ray projection lithography system," J. X-Ray Sci. Technol. 3, 194-203 (1992).
4. W. H. Arnold, "Optical lithography: The compe-titor cost models for the 1990s," presented at the DARPA X-Ray Lithography Workshop, Carmel, California, 16 Oct. 1989.
5. SEMATECH Cost of Ownership Model Revision December 1991, Technology Transfer Number 91020473B-GEN, SEMATECH, Inc., Austin, Texas copyright SEMI 1986, 1990.
6. J. Schroeter, Surviving the ASIC Experience (Prentice Hall, Englewood Cliffs, New Jersey, 1992).
7. V. Di Milia, J. R. Maldonado, J. L. Speidell, and J. M. Warlaumont, U. S. Patent Number 4,551,192.
8. M. A. Hartney, "Surface-imaging lithography," in Soft-X-Ray Projection Lithography, Vol. 12 of OSA Technical Digest Series (Optical Society of America, Washington, D.C., 1991), 120-123.
9. W. M. Mansfield, J. E. Bjorkholm, A. A. MacDowell, R. R. Freeman, L. H. Szeto, G. N. Taylor, D. M. Tennant, W. K. Waskiewicz, D. L. Windt, D. L. White, O. R. Wood II, R. M. D'Souza, and A. R. Neureuther, "Effects of absorption on resist performance in soft-x-ray projection lithography," in Soft-X-Ray Projection Lithography, Vol. 12 of OSA Technical Digest Series (Optical Society of America, Washington, D.C., 1991), 129-131.
10. J. M. Calvert, "Lithographically patterned self-assembled film," to be published in J. Vac. Sci. Technol. B, Nov/Dec, 1993.
11. N. Koshiba of UCB JSR Electronics, private communication.
12. D. L. White, J. E. Bjorkholm, J. Bokor, L. Eichner, R. R. Freeman, T. E. Jewell, W. M. Mansfield, A. A. MacDowell, L. H. Szeto, D. W. Taylor, D. M. Tennant, W. K. Waskiewicz, D. L. Windt, O. R. Wood, II, "Soft x-ray projection lithography," Solid State Technol. 34, 37-42 (1991).

13. K. Early, D. M. Tennant, D. Y. Jeon, P. P. Mulgrew, A. A. MacDowell, O. R. Wood II, G. D. Kubiak, and D. A. Tichenor, "Characterization of AZ PN114 resist for soft-x-ray projection lithography," to be published in Appl. Opt. 32, special issue on SXPL.
14. W. C. Sweat of Sandia National Laboratory, private communication.
15. W. C. Sweatt, "High-efficiency condenser for illuminating a ring field," presented at the OSA SXPL Topical Meeting, May 10-12, 1993, and to be published by the OSA as part of the proceedings.
16. J. B. Murphy, D. L. White, A. A. MacDowell, and O. R. Wood II, "Synchrotron radiation sources and condensers for projection x-ray lithography," to be published in Appl. Opt. 32, special issue on SXPL.
17. D. L. White, AT&T Bell Labs, private communication.
18. A. M. Hawryluk, presented at the Soft x-ray project
19. R. D. Watson and R. H. Stulen, "Analysis of thermally induced distortion of optics for soft-x-ray projection lithography," Vol. 12 of OSA Technical Digest Series (Optical Society of America, Washington, D. C., 1991), 37-41.
20. A. M. Hawryluk, Lawrence Livermore National Laboratory, private communication.
21. T. Koide, T. Shidara, K. Tanaka, A. Yagishita, and S. Sato, "In situ dc oxygen-discharge cleaning system for optical elements," Rev. Sci. Instrum. 60, 2034-2037 (1989).
22. T. Harada, S. Yamaguchi, M. Itou, S. Mitani, H. Maezawa, A. Mikuni, W. Okamoto, and H. Yamaoka, "Ultraviolet/ozone cleaning of a soft x-ray grating contaminated by synchrotron radiation," Appl. Opt. 30 (1991) 1165-1168.
23. A. A. MacDowell, AT&T Bell Laboratories, private communication.
24. "The Semiconductor Technology Workshop Conclusions" (Semiconductor Industry Asso-ciation, San Jose 1993).