Gate Leakage Tolerant Circuits in Deep Sub-100nm CMOS Technologies

Sung-Mo Kang, Ge Yang, and Zhongda Wang
University of California, Santa Cruz
Department of Electrical Engineering
1156 High Street, Santa Cruz, CA 95064
kang@soe.ucsc.edu

ABSTRACT

The leakage power consumption in deep sub-100nm CMOS systems is projected to become a significant part of the total power dissipation. Although the dual Vt CMOS process helps reduce the subthreshold leakage current, the gate leakage problem poses a significant design challenge. We introduce gate leakage tolerant circuits. We describe two new circuit techniques to suppress gate leakage currents in dual Vt Domino circuits. In standby mode, proposed circuits generate low inputs and low outputs for all Domino stages to suppress gate leakage currents in the NMOS logic tree. Simulation results using 45nm BSIM4 SPICE models for 32-bit adders show that adders using the two proposed circuits can reduce the standby gate leakage by 66% and 90%, respectively. Proposed adders have 7% active power overhead to achieve the same speed as single Vt domino adder and the area penalty is minimal with careful layout.

1. INTRODUCTION

Scaling down supply voltage is known to be the most effective way to reduce power consumption. For lower power supply voltage, the threshold voltages of transistors also need to be scaled down to meet the performance requirements. However, the lowering of threshold leads to the exponential growth of the subthreshold leakage current. Thus, dual-threshold voltage techniques [1, 2] have been used to solve this dilemma.

As CMOS process advances to sub-100nm regime, the gate oxide thickness gets scaled down to sub-20 Å [3]. Such thin oxide leads to significant gate leakage currents by various direct tunneling mechanisms [4]. And gate leakage is projected to be the dominant factor for sub-100nm generations [5]. Gate leakage models for MOSFET have been proposed [6, 7], and device and circuit level schemes to reduce gate leakage have been proposed [8, 9, 10].

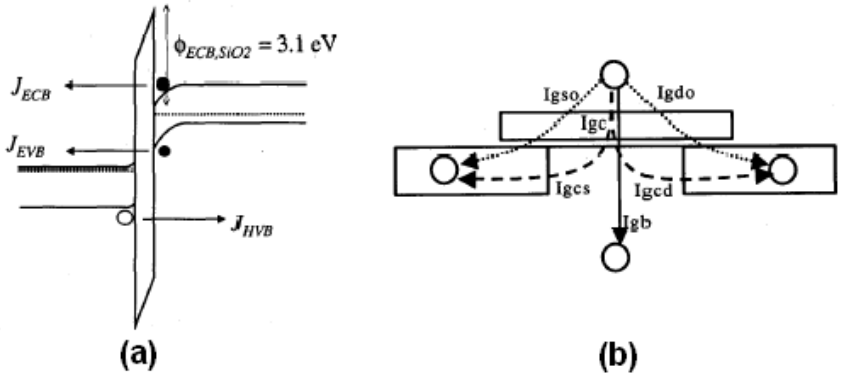


Figure 1 (a) Three mechanisms of gate dielectric direct tunneling leakage; (b) Components of tunneling current [7]

Figure 1(a) shows the three major gate leakage mechanisms for MOS structures, namely electron conduction-band tunneling (ECB), electron valence-band tunneling (EVB), and hole valence-band tunneling (HVB). Figure 1(b) shows the components of the gate tunneling current. I_{gb} is the gate-to-substrate leakage current; I_{gso} and I_{gdo} are parasitic leakage currents through gate-to-S/D extension overlap region; and I_{gc} is the gate-to-inverted channel tunneling current. Part of I_{gc} is collected by the source (I_{gcs}) while the rest goes to the drain (I_{gcd}) [7].

In this paper, we introduce two new circuit techniques developed to suppress the gate leakage in dual Vt domino circuits. The effectiveness of the proposed circuits is verified by simulation results for a domino OR gate and 32-bit

Microelectronics: Design, Technology, and Packaging, edited by Derek Abbott, Kamran Eshraghian, Charles A. Musca, Dimitris Pavlidis, Neil Weste, Proceedings of SPIE Vol. 5274 (SPIE, Bellingham, WA, 2004) · 0277-786X/04/$15 · doi: 10.1117/12.530278

adders using 45nm BSIM4 models [13]. The rest of this paper is organized as following. Section 2 evaluates prior art. Section 3 presents the gate leakage study of domino circuit. Section 4 introduces new circuits for leakage-proof domino. Simulation results are shown in Section 5, followed by summary in Section 6.

2. PRIOR ART

2.1 Boosted Gate MOS (BGMOS)

Inukai et al. proposed a device/circuit cooperation scheme, called boosted gate MOS (BGMOS), as shown in Figure 2 [8]. Low Vt transistors with thin T_{ox} are used for the core circuit, while transistors with higher Vt and thicker T_{ox} are used as low leakage switches to suppress the subthreshold leakage and gate leakage in sleep mode. A boosted gate voltage is applied to transistors with higher Vt and thicker T_{ox} to reduce the area penalty. This scheme requires dual supply voltages and fabrication process to achieve dual T_{ox}.

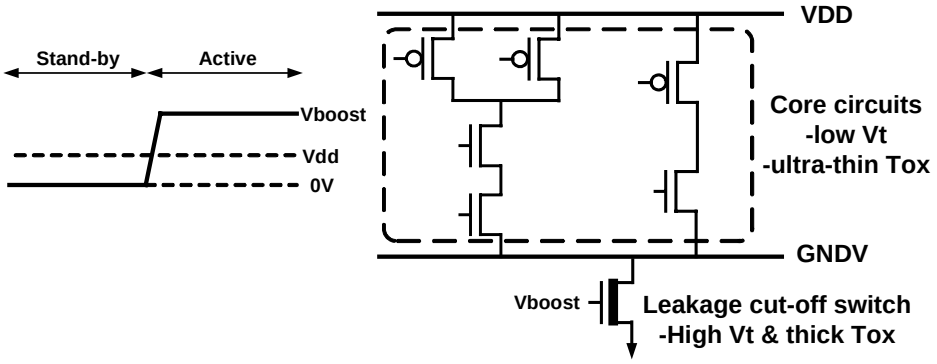


Figure 2: Boosted Gate MOS

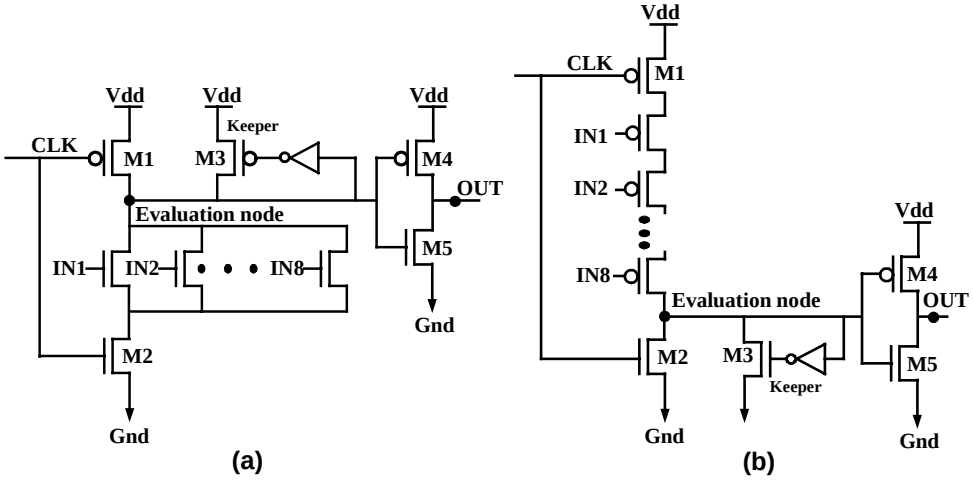


Figure 3: (a) N-type 8-input domino OR gate; (b) P-type 8-input domino OR gate

2.2 P-type domino

Hamzaoglu et al. proposed a P-type domino, which uses PMOS transistors in the logic tree instead of NMOS transistors [9]. It is based on the fact that, under inversion bias, gate leakage through SiO_2 for PMOS transistors is an order of magnitude lower than that of NMOS transistors [11]. The difference can be explained as following. The electron tunneling from conduction band (ECB) is the dominant component of gate leakage for NMOS transistor, whereas the hole tunneling from valence band (HVB) is for PMOS transistor. As the barrier height for HVB is significantly bigger than the barrier height for ECB, gate leakage for PMOS transistor is much lower [11]. On the other

hand, the PMOS transistors in the logic tree of a P-type domino have to be up sized to achieve the same performance as N-type domino, due to lower mobility of holes. This will increase the area and active power consumption. High fan-in domino gates are often employed in performance critical units of microprocessors and other high performance VLSI circuits [12]. OR function is performed by parallel connected NMOS transistors for the N-type domino as shown in Figure 3(a), while it is performed by serial connected PMOS transistors for the P-type domino as shown in Figure 3(b). In sum the P-type domino loses its advantage for high fan-in dynamic gates used for high performance.

2.3 State-dependent Gate Leakage Table

Guindi et al. showed that the total gate leakage in a given structure varies significantly for different combinations of inputs, from which they derived "state-dependent gate leakage tables" that can be used to estimate the total amount of the gate leakage current for a large circuit [10]. Figure 4 shows the gate leakage currents in the NAND gate for different input patterns.

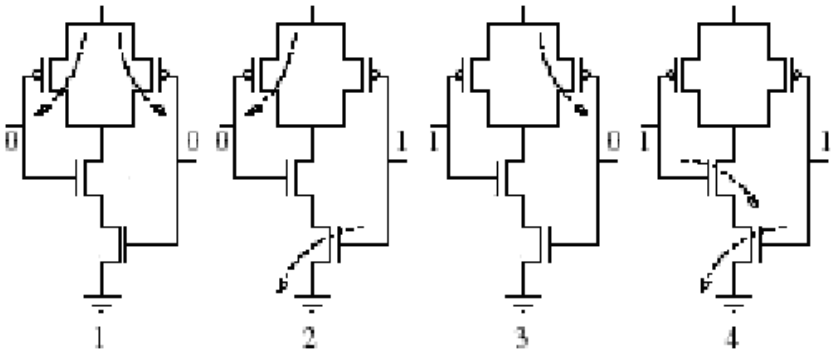


Figure 4: Gate leakage for the different states in a 2-input NAND gate [10]

Table 1 shows the normalized total gate leakage per state for a 2-input NAND gate and a 2-input NOR gate. Gate leakage in PMOS transistor was assumed to be one tenth of that in NMOS transistor. Unsized transistors were assumed to have equal minimum-sized NMOS and PMOS transistors, whereas sized gates were designed for equal rise time and fall times. Note that symmetrical input (0 1) and input (1 0) do not produce the same amount of leakage as shown in Table 1. We could assign the input signals in a way that favors the low leakage state if we know the signal switching probabilities. The state-dependent gate leakage tables can be used to find an input pattern for a large circuit to achieve low gate leakage state during standby.

Table 1: Normalized state-dependent gate leakage in NAND and NOR gates [10]

Input	NAND		NOR	
	Unsized Wn=1X Wp= 1X	Sized Wn=2X Wp= 3X	Unsized Wn=1X Wp= 1X	Sized Wn=1X Wp= 6X
0 0	0.2	0.6	0.2	1.2
0 1	1.1	2.3	1	1
1 0	0.1	0.3	1.1	1.6
1 1	2	4	2	2

3. LEAKAGE STUDY OF DOMINO OR GATE

To address gate leakage problem, we chose 45nm BSIM4 models [13]. BSIM4 has an accurate gate direct tunneling model and a gate-induced drain leakage (GIDL) current model [14]. The parameter "IGCMOD" in the model is the gate-to-channel tunneling current model selector and the parameter "IGBMOD" in the model is the gate-to-substrate tunneling current model selector. We can set both parameters to "0" or "1" to exclude or to include gate leakage in the simulation.

3.1 Gate leakage of devices

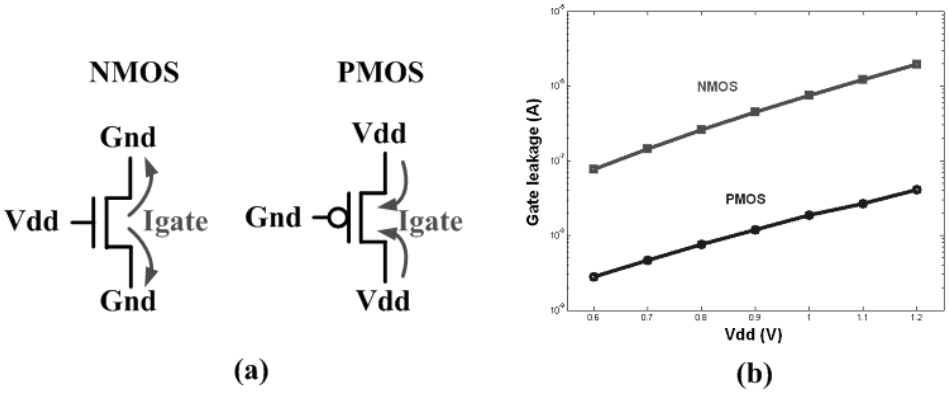


Figure 5 (a) Transistor connection for gate leakage measurement (b) Gate leakage of NMOS and PMOS transistors

Figure 5(a) shows terminal connections for gate leakage measurement of NMOS and PMOS transistors. The gate of the NMOS transistor is connected to the power supply Vdd, while the drain and source are connected to the ground Gnd. For PMOS transistor, the gate is connected to the ground, while the drain and source are connected to the power supply. Gate leakage currents flow as shown in Figure 5(a). The electrical equivalent gate oxide thickness (Toxe) of 1.4nm was used for both NMOS and PMOS transistors for simulation [3, 12]. The width and length of both NMOS and PMOS transistors were set to be 1um and 0.045um, respectively. Simulation results in Figure 5(b) confirm that the gate leakage of NMOS transistor is more than an order of magnitude higher than that of PMOS transistors. The gate leakage is 260nA for NMOS transistor, while it is 7.6nA for PMOS transistor when Vdd is 0.8V.

3.2 Single Vt domino

An eight-input single Vt domino OR gate shown in Figure 6 is used as test circuit. We first performed simulation to observe the impact of gate leakage on the performance of domino circuit. In this case, the gate leakage is negligible compared to the drain current when the transistor is on, and thus its impact on performance is negligible. Performance degradation due to gate leakage is less than 0.1% when the power supply equals 0.8V [3]. Simulation also shows that gate leakage currents have little impact on dynamic power consumption.

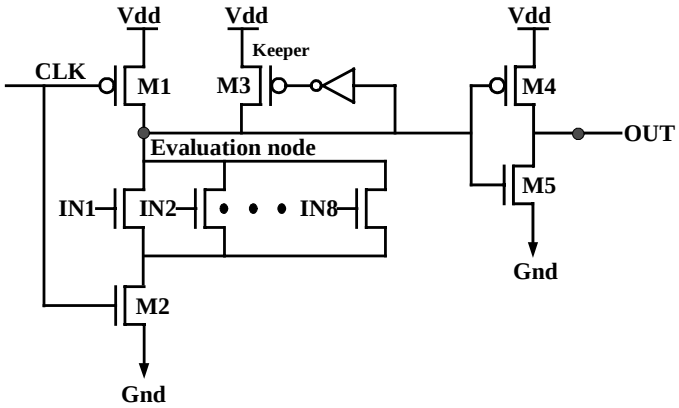


Figure 6. Single Vt 8-input domino OR gate

Figure 7 shows the leakage currents in the domino OR gate in standby mode. The gate leakage increases quickly with the increase of the power supply voltage. It exceeds the subthreshold leakage for the power supply voltage greater than 0.7V, and almost of equal amount at below 0.7V.

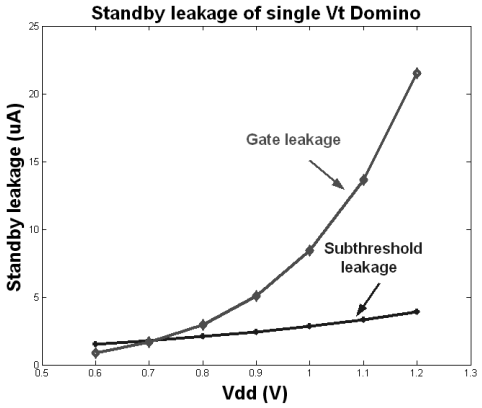


Figure 7. Standby leakage of single Vt Domino

3.3 Dual Vt Domino

Dual Vt techniques have been used for domino circuits to suppress the subthreshold leakage [1, 2]. Figure 8 shows the dual Vt implementation of the circuit in Figure 6. The parameter "Vth0" in the 45nm BSIM4 model is 0.22V for NMOS and -0.22V for PMOS. For high Vt devices, we have set the parameter "Vth0" to 0.35V for high Vt NMOS and -0.35V for PMOS.

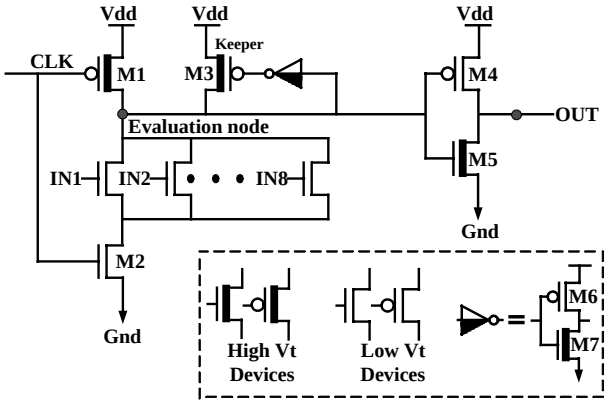


Figure 8. Dual Vt 8-input domino OR gate

Transistors M1, M3, M5 and M7 shown in Figure 8 are high Vt devices. They are in the non-critical path of the circuit, thus the performance will not be degraded. In standby mode, the clock signal and inputs to the domino circuit should be high [2][15]. The high clock signal turns off transistor M1. The NMOS logic tree with high inputs discharges the evaluation node, which turns off transistors M5 and M7. Discharged evaluation node turns on transistor M6, and M6 turns off transistor M3. Then all the high Vt devices are turned off to suppress the subthreshold leakage. The output of the dual Vt domino is high in standby mode and this ensures that the succeeding domino stages will be biased into the low subthreshold leakage state.

For multi-stage domino circuits, if the inputs to the first stage are not set high, the evaluation node of the first domino stage will be discharged slowly by the leakage current. This may lead to a short circuit current flowing through the output inverter of the domino circuit. Thus a gating stage is required for the first domino stage to set all the inputs high in standby mode to bring all the domino stages into low leakage state quickly without short circuit current in the

domino output inverter [2, 14]. Figure 9 shows the multi-stage dual Vt domino circuits with gating stage. The high inputs and outputs of all stages together with the high clock signal bias the circuits into low subthreshold leakage state.

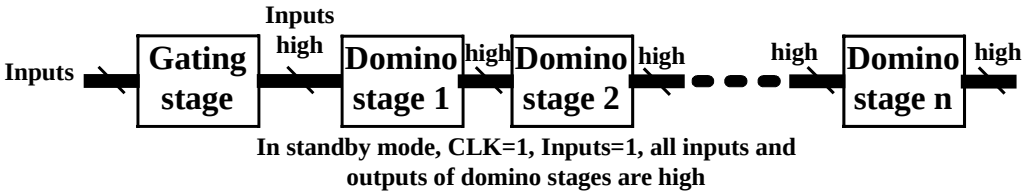


Figure 9. Multi-stage dual Vt domino circuits with gating stage in standby mode

Although subthreshold leakage current is reduced by high Vt devices in dual Vt domino circuits in standby mode, their gate leakage is not. Figure 10 shows that standby gate leakage is about two orders of magnitude larger than the subthreshold leakage in a dual Vt domino circuit at the 45nm node. And the gate leakage mainly comes from the NMOS logic tree. Special process techniques or circuit techniques need to be developed to address this gate leakage problem.

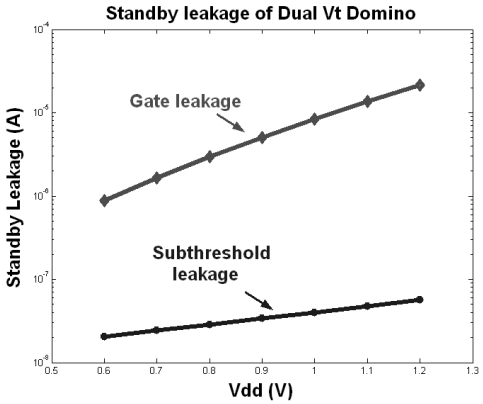


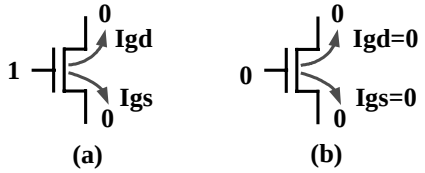
Figure 10. Standby leakage of dual Vt Domino

4. NEW CIRCUIT DESIGN FOR LEAKAGE-PROOF DOMINO

4.1 Basic Idea of Suppressing Gate Leakage

In conventional dual Vt domino logic, inputs and outputs of every domino stage are set high in standby mode as shown in Figure 9. The gate of the transistors in the NMOS logic tree is high, while the source and drain nodes of those transistors are low, gate-to-drain and gate-to-source tunneling currents flow in those NMOS transistors in standby mode as shown in Figure 11(a).

If we can set the gate, drain and source voltages of the transistors in the NMOS logic tree are all low as shown in Figure 11(b), there will be no gate leakage in the NMOS logic tree. Thus, for leakage-proof domino circuits in deep sub-100nm technologies, all inputs and outputs of domino stages should be low to suppress gate leakage in standby mode. Also all high Vt devices should be turned off by some means to suppress the subthreshold leakage. The gating stage should also be avoided to save area and active power consumption, without the penalty of the short circuit current in the domino output inverter when entering the standby mode. Figure 11(c) shows the desirable multi-stage leakage-proof domino circuits in standby mode.



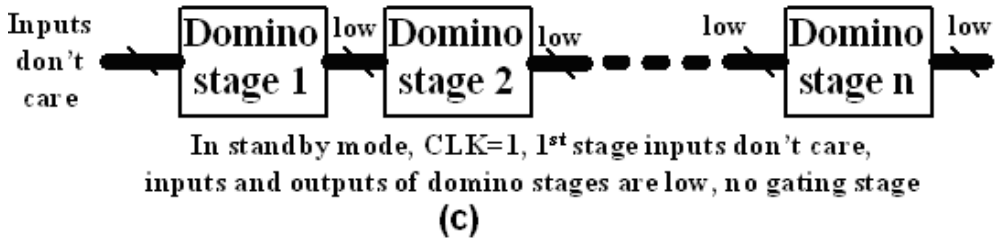


Figure 11. (a) Gate leakage in NMOS; (b) No gate leakage; (c) Multi-stage leakage-proof domino circuits in standby mode

4.2 Proposed Circuit I

We have developed two new versions of domino circuit to reduce both the subthreshold leakage and the gate leakage. The first version is shown in Figure 12. Three transistors M8, M9 and M10 are added to the conventional dual Vt domino.

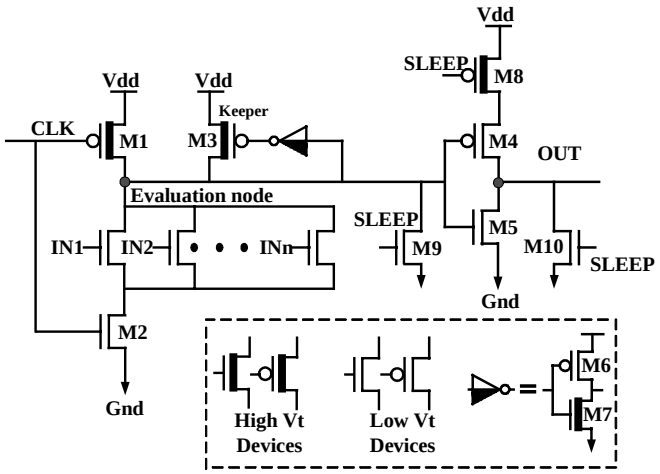


Figure 12. Proposed circuit I

4.2.1 Operation mode

In operation mode, SLEEP is low. M9 and M10 are off and M8 is on. The proposed circuit works like the conventional dual Vt domino.

4.2.2 Standby mode

In standby mode, CLK and SLEEP are high. M1 and M8 are turned off by CLK and SLEEP. NMOS sleep transistor M9 is turned on by high SLEEP. It discharges the evaluation node to ground and the discharged evaluation node turns off high Vt devices M3 and M7. All potential subthreshold leakage paths are then suppressed by turned off high Vt devices M1, M3, M7 and M8.

The gate, drain and source nodes of the NMOS transistors in the NMOS logic tree are all set low as shown in Figure 11(b). Thus, there is no gate leakage in the NMOS logic tree. NMOS sleep transistor M10 is turned on by high SLEEP to discharge the domino circuit output so that inputs to the next stage domino circuits are low. The inputs and outputs of all domino stages are all low as shown in Figure 11(c). Thus no gate leakage flows in the NMOS logic tree in standby mode.

The gating stage can be avoided due to the use of transistor M9. No matter what the inputs to the first domino stage, the evaluation node can be discharged by transistor M9.

4.3 Proposed Circuit II

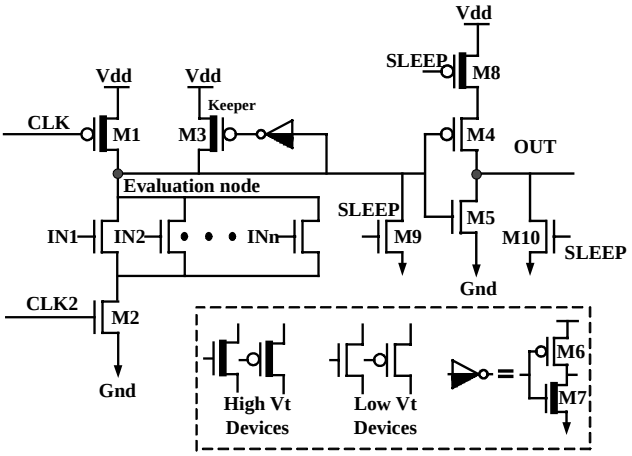


Figure 13. Proposed circuit II

Figure 13 shows the second version. The only difference from the first version is that two clock signals are used in this circuit. CLK2 is the same as CLK in operation mode, but CLK2 is low in standby mode while CLK is high. This configuration turns off the foot clock NMOS M2 in standby mode to further reduce the gate leakage.

5. SIMULATION RESULTS

We simulated 8-input domino OR gate and 32-bit carry lookahead adders to verify the proposed circuits. 45nm BSIM4 models [13] were used in our simulation and the power supply was 0.8V [3].

5.1 8-input domino OR gate

We simulated three 8-input dual Vt domino OR gates using conventional dual Vt domino and the two proposed circuits. The gating stage for multi-stage dual Vt domino circuits is not considered here, and this simulation case is to show the effectiveness of proposed circuits to suppress gate leakage. All three gates were tuned to operate at 1GHz clock frequency.

Table 2 shows the simulation results. The delay, active power consumption and the standby gate leakage current of the 8-input dual Vt domino gate using conventional domino circuit are normalized to unity.

Table 2: Simulation results of 8-input domino OR gate

	Normalized delay	Normalized active power	Normalized standby gate leakage
Dual Vt domino	1	1	1
Proposed I	1	1.06	0.13
Proposed II	1	1.06	0.01

Proposed circuit I reduces gate leakage by 87% over the conventional dual Vt domino circuit. Proposed circuit II further suppresses the gate leakage by turning off the clock NMOS M2 in standby. Thus the second circuit version reduces gate leakage by 99% over the conventional dual Vt domino circuit.

The active power consumption of both proposed circuits is 6% more than the conventional dual Vt domino power. This is due to the serially connected PMOS transistors M4 and M8 in Figure 8 and Figure 9. To achieve the same performance as conventional dual Vt domino, M4 and M8 have to be up sized, which increases the capacitance at the evaluation node. Thus the switching power at the evaluation node is increased.

The delay of a domino gate is the delay of the evaluation node discharge plus the delay of the output node pulling up. Upsizing of the PMOS M4 will cause slow transition of the evaluation node due to increased capacitance, but it will

speed up the pulling up of the evaluation node. The upsizing of transistors M4 and M8 could be tuned no to have delay penalty.

Area penalty of proposed circuits is minimal with careful layout. NMOS transistor M9 and M10 shown in Figure 12 and Figure 13 are small size transistors. The main area penalty comes from the up sized M4 and M8 in Figure 12 and Figure 13 to match the same performance of the conventional domino. The total transistor width of NMOS transistors is larger than that of PMOS transistors in domino circuit due to the NMOS logic tree. Thus, there is always some spare space in the layout for PMOS transistors. The upsized PMOS M4 and M8 can be placed in the spare area with careful layout.

The penalty of routing for CLK2 in the second proposed circuit is neglected in the simulation.

5.2 32-bit carry lookahead adders

We designed four carry lookahead adders using single Vt domino, dual Vt domino and the two proposed circuits. All four adders were tuned to achieve 1GHz clock frequency operation. The adder structure introduced in [16][17] requires much less interconnect wiring than Kogge-Stone adder structure [18], thus less layout area and less power consumption. We adopted this new adder structure for low power consideration.

Table 3: Simulation results of 4 adders

	Clock Frequency	Active power	Standby leakage		
			I_{sub}	I_{gate}	I_{total}
Single Vt	1GHz	14.1mW	985uA	728uA	1.71mA
Dual Vt	1GHz	15.8mW	44.3uA	750uA	794uA
Proposed I	1GHz	15.1mW	41.4uA	246uA	287uA
Proposed II	1GHz	15.1mW	41.4uA	75.1uA	116uA

The simulation results of the four adders are shown in Table3. The penalty for routing of CLK2 of the second proposed circuit was neglected in the simulation. All four adders achieve maximum operating clock frequency of 1GHz. The single Vt domino adder consumes 14.1mW active power, and its total leakage current in standby mode is 1.71 mA. 58% of the total leakage current is the subthreshold leakage and 42% is the gate leakage. Dual Vt domino adder consumes 15.8mW active power, 12% more than the single Vt domino adder due to additional gating stage. The subthreshold leakage current in dual Vt domino adder is only 5% of that in the single Vt domino adder. And the gate leakage contributes to 95% of the total leakage current of the dual Vt domino adder. Proposed circuit I reduces 96% of the subthreshold leakage current and 66% of the gate leakage, compared to the single Vt domino adder. Proposed circuit II reduces 96% of the subthreshold leakage current and 90% of the gate leakage, compared to the single Vt domino adder. Figure 14 shows the normalized leakage currents in the four adders.

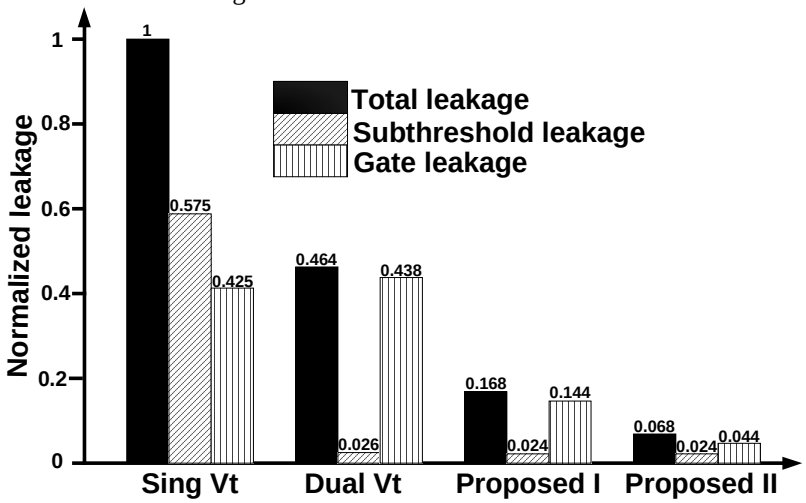


Figure 14. Normalized leakage current of 4 adders in standby mode

Proposed circuits consume 7% more active power than the single Vt domino adder due to the upsizing of the PMOS transistor in the domino output inverter for no delay penalty purpose. The two adders using proposed circuits could be biased into the low leakage state in 0.5ns, and the energy consumed for transition from operation mode to standby mode due to the switching of the gates of the sleep transistors is 0.137pJ. Sleep transistor M8 in Figure 12 and Figure 13 can be shared by all the domino stages in the same row. And the sleep transistors can be distributed uniformly across the adder layout to prevent undesirable current crowding in the power grids [19]. Dual Vt domino adder also need sleep signal in its gating stage, and the energy consumed for transition from operation mode to standby mode is 0.106pJ.

Both the dual Vt domino adder and proposed adders consume more active power than the single Vt domino adder, although they have less leakage current in standby mode. To better evaluate the effectiveness of the proposed circuits, we compare the total power consumption of the four adders. We define the idle rate R_{idle}, and the total power consumption P as:

$$R_{idle}=T_{idle}/T_{total} \quad (1)$$

$$T_{total}=T_{idle}+T_{active} \quad (2)$$

$$P = P_{active}\bullet (1-R_{idle})+ P_{idle}\bullet R_{idle} \quad (3)$$

Where T_{idle} is the amount of time in standby mode, T_{active} is the amount of time in operation mode, P_{idle} is the power consumption in standby mode, and P_{active} is the power consumption in active mode. Using Equations (1)-(3) and simulation results in Table 3, we can calculate the total power saving of proposed adders over the single Vt domino adder and the dual Vt domino adder. The results are shown in Figure 15. The total power saving increases with the idle rate. We can see from Figure 15(a) that at the idle rate of 0.95, adders using proposed circuits will have 52% and 58% total power saving respectively, compared to the single Vt domino adder. At the same idle rate, the total power saving of proposed adders over the dual Vt domino adder are 30% and 40% respectively, as shown in Figure 15(b).

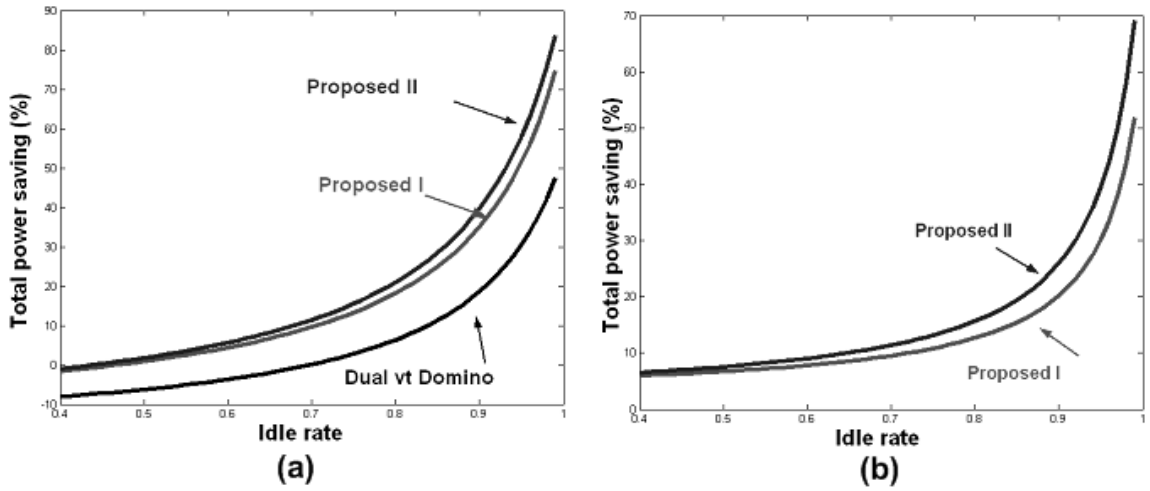


Figure 15. (a) Total power saving over single Vt domino adder; (b) Total power saving over dual Vt domino adder

The total power saving of the dual Vt domino adder over the single Vt domino adder is positive for the idle rate greater than 0.70. Adders using proposed circuit I and proposed circuit II will have positive total power saving for idle rate greater than 0.47 and 0.44, respectively. The proposed circuits have a larger range of idle rate for positive power saving and they would help reduce the overall power consumption of battery operated portable devices.

SUMMARY

Both the subthreshold leakage current and the gate leakage current should be suppressed in deep sub-100nm CMOS technologies for low power consumption. We have reviewed gate leakage tolerant circuits and we have proposed two leakage-proof domino circuits. Simulation results for 32-bit adders show that adders using the two proposed circuits reduce the total standby leakage by 83% and 93%, respectively, compared with the adder using single Vt domino circuits for the predictive 45nm technology. Other than 7% increase in the active power, there is no overhead in delay and the area penalty is minimal with careful layout. We have shown that the total power saving increases as the idle rate of domino logic increases.

ACKNOWLEDGMENTS

This research was supported in part by Semiconductor Research Corporation under contract 2001-HJ-891 and Intel Corporation.

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