A Year in the Life of an Immersion Lithography Alpha Tool at Albany NanoTech

Michael Tittnich[1], John Hartley[1], Greg Denbeaux[1]
Uzo Okoroanyanwu[2], Harry Levinson[2]
Karen Petrillo[3], Chris Robinson[3], Dario Gil[3], Dan Corliss[3]
David Back[4], Stefan Brandl[4], Christian Schwarz[4], Frank Goodwin[4], Yayi Wei[4], Brian Martinick[4]
Richard Housley[5], Peter Benson[5]
Kevin Cummings[6]

[1]College of Nanoscale Science and Engineering, University at Albany, NY
[2]Advanced Micro Devices
[3]IBM
[4]Infineon Technologies
[5]Micron Technology
[6]ASML

Immersion Lithography continues to get more and more attention as a possible solution for the 45nm technology node puzzle. In 2005, there has, indeed, been a lot of progress made. It has gone from a laboratory curiosity to being one of the industry's prime contenders for the lithography technology of choice for the 45nm node. Yet a lot of work remains to be done before it's fully implemented into production. Today, there are over a dozen full field immersion scanners in R&D and pilot lines all around the world. The first full field, pre-production "Alpha" version of the ASML Twinscan AT 1150i was delivered to Albany NanoTech in August, 2004. A consortium made up of AMD, IBM, Infineon, and Micron Technology began early evaluation of immersion technology and in December of 2004, the production of the world's first Power PC microprocessor using immersion lithography, processed on this tool, was announced by IBM.
This paper will present a summary of some of the work that was done on this system over the past year. It will also provide an overview of Albany NanoTech, the facility, its capabilities, and the programs in place. Its operating model, which is heavily focused on cooperative joint ventures, is described. The immersion data presented is a review of the work done by AMD, IBM, Infineon Technologies, and Micron Technology, all members of the INVENT Lithography Consortium in place at Albany NanoTech. All the data was published and presented by the authors in much more detail at the 2005 International Symposium on Immersion Lithography, in Bruges, Belgium.

The Albany NanoTech Facility and Operating Model

The State of New York has established a comprehensive, integrated, state technology development strategy. Central to this strategy is a $1.5B program to create a number of technical "Centers of Excellence" throughout the State University system. Albany NanoTech, together with the College of Nanoscale Science and Engineering, at the State University of New York at Albany, make up the NYS Center of Excellence in NanoElectronics. The college was the first in the nation

Emerging Lithographic Technologies X, edited by Michael J. Lercel,
Proc. of SPIE Vol. 6151, 615101, (2006) · 0277-786X/06/$15 · doi: 10.1117/12.663785

to establish comprehensive, advanced degree programs focused specifically on nanotechnology. Albany NanoTech is an international R&D resource for academic and industrial NanoElectronics communities.

The first 200mm semiconductor research facility, NanoFab 200, was completed in 1996. In 2003, a 300mm facility, NanoFab 300 South, was constructed with a total of 17,000 sq. ft. of clean room space. An annex of an additional 14,000 sq ft of cleanroom was added in February of 2004. Construction of a third, 300mm facility was finished in the fall of 2005, and the first equipment was delivered in December, 2005. Plans are in place for a fourth cleanroom and office complex to be built on the site, with ground breaking expected later this year. Albany NanoTech provides the entire state of the art infrastructure to support a "shared use, co-location" model used by a consortia of international semiconductor device and equipment suppliers. These partners include SEMATECH, IBM, AMD, Micron Technology, Infineon, Applied Materials, Tokyo Electron, and ASML. There is a total of 750,000 sq. ft of leading edge facilities with 68,000 sq. ft cleanroom space.

The keystone of the organization is the NYS Center of Excellence for NanoElectronics, a partnership between Albany NanoTech and the College of Nanoscale Science and Engineering at the State University of New York (CNSE). The partnerships that have been established around the Center of Excellence provide significant engineering resources to help drive the development programs, each one established independently, but working together to synergistically leverage the total resource base of the Center. SEMATECH North encompasses the EUVL Mask Blank Development Center and the SEMATECH Resist Test Center. The Mask Blank Development Center is the leading R&D center of its kind, in the world. The Resist Test Center focuses on EUV and Hyper NA 193nm immersion Photoresist evaluation and development.

The International Nanoelectronics Venture (INVENT), a joint research and development consortium, was formed in 2003 between CNSE, AMD, IBM, Infineon, and Micron Technology. The initial focus of this consortium was the development of 157nm and EUV lithography technology for the semiconductor industry. 193nm immersion lithography has since replaced the 157 program.

Tokyo Electron, Ltd. established the TEL Technology Center of America (TTCA) in 2003. TTCA focuses on semiconductor equipment and process development. It is the primary R&D facility for Tokyo Electron outside of Japan. In 2005, Applied Materials, IBM, and CNSE formed a joint venture to work on the development of new materials, processes, and equipment for the semiconductor industry. Also in 2005, the International Multiphase Program for Lithography Science and Engineering (IMPLSE) was formed between ASML, IBM, and CNSE to further expand the photo lithography base of the center. When fully staffed, this will be the largest technology development center for ASML outside of the Netherlands. Together, all these programs make up one of largest and most advanced semiconductor research centers in the world.

The core of this semiconductor R&D operation will be the Center for Semiconductor Research (CSR), a joint venture led by Albany NanoTech and IBM, leveraging the resources of existing programs to establish a CMOS research line to develop 32nm, and beyond, technologies. The CSR combines the resources and capabilities of the various consortia in Albany to enable integrated processing, yet allowing the individual companies to carry out their own, proprietary R&D programs. The CSR will house over 125 state of the art; 300mm process tools when full build out is completed. Tool

hook-up and qualification of Phase 1 will be completed by the end of Q3, 2006. The line is designed for the 32nm node and beyond, but will be compatible with previous generations of technology. It will have unit process, module integration, and full flow capabilities. A 45nm baseline process will be run for line monitoring and for use by all our partners. It has an initial capacity of 25 integrated wafer starts per day and will operate 24X7 on a low volume, rapid turn around time model to speed cycles of learning. Albany NanoTech will provide all the facilities, some of the process tools and engineering resources, a portion of the operating expenses, and operates the facility. Our partners provide engineering resources, some process tools, process technology IP for joint programs and for their own, proprietary programs, and a portion of the operating expenses. Other parties can participate as partners in specific programs, or on a customized individual use basis. This model provides a highly leveraged cost structure, and maximum flexibility, the perfect environment in which to install and evaluate a high cost, high risk, first of a kind Alpha tool.

Lithography Programs

The lithography equipment in place currently are an ASML Twinscan AT 1150i and AT 1200B. In Q3, 2006, a Twinscan XT1700i will be installed. We actually still have installed in the clean room an ASML Micrascan 7. The 157nm technology development program was not exactly a success story for the semiconductor industry. Fortunately, for the members of INVENT, the costs were shared across the program, and Albany NanoTech funded a large portion of the program. Individual company financial exposure was low. And, even when a technology development program is successful, as it was with 193nm lithography, there is still a high cost of early adoption and alpha tool evaluation. Most of the early 193 alpha tools were used for only a short time before they were replaced by higher NA, more capable scanners. Most of them ended up listed for sale on equipment re-marketing web sites, for pennies on the dollar, and there weren't many takers. Most of them are still there. Yet the need for active customer involvement early in the development phase of this equipment cannot be overlooked. The early learning for the user in developing processes, and the feed back required by the supplier to enable improvements in the equipment technology is critical. But, the cost of developing new technology is only going up, along with the risk. The best approach is through a consortium of users, equipment suppliers, universities and government. In an environment where costs and risks are shared, where the possibility exists to provide funding for equipment development and no one company bears the sole financial burden. Where companies can work together, jointly, in a pre-competitive mode, or privately, as the need arises.

The other lithography systems in place today at Albany NanoTech are the SEMATECH North program Exitech MS13 EUV and Hyper NA 193 immersion steppers. CNSE operates a stand alone, EUV source from Energetiq Technology, used for actinic wavelength metrology projects, EUV resist out gassing evaluation, hardware contamination and other studies. A direct write E-beam program and a Nano Imprint program are in the early stages of negotiation. Later this year we will take delivery of one of the first ASML EUVL Alpha Demo tools, and our work on Alpha tool evaluation begins again.

Immersion Lithography Evaluation

It's been shown that there is a real process window improvement gained from increased depth of focus (DOF) with immersion lithography. DOF = (immersion index)*wavelength/ (N.A.) ^2, where N.A. is the numerical aperture. For a refractive index of water (1.44) relative to the refractive index of air (1.0), a 44% effective increase in the DOF can be realized. (Figure The real question now is can we control and eliminate defects so it can be used in production.

The concern with defects started with the water. Immersion lithography doesn't employ a controlled drying process as in other wet processes in the fab. Residual water was allowed to evaporate, which led us to believe there was a need for cleaner UPDI water. We installed a second, in-line polishing skid to provide the highest quality water possible. Methods were devised to periodically test the water at various points. A sanitization processes was developed to remove any trace of bacteria, including anywhere in the immersion system itself. (Figure 1.)

ASML designed and installed the Water Immersion Control Cabinet to control the water within the scanner. It provided additional temperature control, filtration, and the ability to further de-gasify and re-gasify the immersion water. It has since been re-packaged, and re-designed. Significant work has been done to improve its ability to customize the condition of the water.

As the INVENT consortium began evaluating the immersion system performance, higher levels of defects were observed than could be attributed to the water alone. (Figure 2.) Work started immediately to determine the source of the added defects.

Extensive research has been done at the University of Wisconsin on the effects of stage velocity on receding dynamic contact angles and water loss from the immersion envelope[1]. Initial work focused on the possible presence and evaporation of residual water droplets and its effect on defectivity. Evidence gathered showed that evaporation of water droplets left behind the scanning trail was a viable source of added defects[2]. The elimination of this residual water is important, as it has also been shown that there is an interaction between the water and the resist and top coat which will leave a residue behind. Residues were observed on all materials tested in this experiment, but whether or not these residues result in patterned defects needs further work[2]. ASML used the data generated on evaporation related defects to make significant improvements in the immersion head design, in the exposure chuck, and the wafer exposure environment to greatly reduce this effect. Wafer surface condition effects caused by the choice of resist / topcoat combination are better understood, and can be controlled to minimize the defects.

Bubbles have been a concern since the introduction of the immersion concept. The source and impact of bubble formation was also investigated. It was hypothesized that bubble formation was a function of stage scan speed, wafer surface condition, resist outgassing, and water quality. Bubbles that adhere to the wafer surface during exposure will, theoretically, act as micro lenses and magnify and distort the image. This was simulated and confirmed in observations made on wafers processed on the ASML Immersion Alpha tool at Albany NanoTech[3].

Evidence showed a strong correlation between high speed scanning and the formation of bubbles and water droplets on the tool. The highest level of defects was observed along the scan trail and at the immersion head entry points at the edge

of the wafer. The impact of stage speed on immersion related defects specifically was presented by AMD and IBM at the 2005 ISIL Conference. As the stage velocity was decreased, defects were reduced correspondingly[2, 3].
All Photoresist in regular use on the ASML Alpha tool at Albany NanoTech used top coats. All materials used underwent a leaching test to ensure minimal exposure of the water to any resist components. The Water Extraction Analysis system used was designed and built by the IBM Almaden Research Center. Although it was believed any components leaching out of the Photoresist would diffuse across the lens / water gap orders of magnitude slower in water than in a gaseous environment, and that the water flow would tend to flush any contaminants away, we chose to be conservative and take no chance in damaging the lens. We established a maximum level of 5 ppb, total sulfonates, in order for a material to be used with no limits. The maximum allowable level was raised for low usage materials. The interactions between the resist and top coats were studied and compatibility was assessed. Not all resist / top coat combinations were compatible. The resist loss on the exposed wafers was determined from cross section measurements after imaging. While most combinations of resists and top coats showed adequate performance, there were some catastrophic failures which showed extreme film loss[4]. A very encouraging result was that no impact to lens performance as indicated by stray light was observed. The ASML SAMOS test was used to measure the stray light levels (Figure 3). We believe we can relax the constraints on the allowable levels of component leaching, and work is continuing with a number of the major Photoresist suppliers to evaluate new Photoresist and top coat materials.
The "Shared-Use, Co-location Model" used by Albany NanoTech has proven to be a cost effective, risk mitigating approach in the evaluation and development of new technology. It provides a state of the art environment that facilitates pre-competitive, cooperative joint ventures between some of the industry's leading semiconductor manufacturers. These joint ventures, combined with the on-site programs established with the world's largest suppliers of semiconductor process equipment can significantly accelerate the development of advanced equipment technology. In this evaluation of the ASML Twinscan 1150i Alpha Immersion Tool, real-time learning on equipment performance was available to ASML from multiple users in a very short time. This knowledge enabled improvements to be made in later versions of ASML immersion scanners in a fast and effective manner.

References

1. Static and Dynamic Contact Angles of Water on Photoresist. H. Burnett, T. Shedd, G. Nellis, and R. Engelstad EIPBN, 2005 and The Effect of Surface Characteristics on Contact Line Motion in Immersion Lithography. H. Burnett , (M. S. Thesis University of Wisconsin, 2004)
2. The Role of Evaporation in Defect Formation in Immersion Lithography. D. Gil, C. Larson, G. Wallraff, R. Allen, C. Robinson, and D. Corliss (IBM) International Symposium on Immersion Lithography, 2005

3. Prospects and Challenges of Defectivity in Water Immersion Lithography. U. Okoroanyanwu, J. Kye, H. Levinson, and N. Yamamoto (AMD); K. Cummings (ASML) International Symposium on Immersion Lithography, 2005
4. Top Coat Compatibility Studies: What you wanted to know about resist / top coat compatibility but were afraid to ask. K. Petrillo (IBM); R. Housley and P. Benson (Micron Technology); F. Goodwin, Y. Wei, S. Brandl, and B. Martinick (Infineon Technologies) International Symposium on Immersion Lithography, 2005
5. Measuring Top Coat Compatibility Using Elipsometry. C. Schwarz, F. Goodwin, and Y. Wei (Infineon Technologies, NA); P. Benson, R. Housley (Micron Technology) International Symposium on Immersion Lithography, 2005
6. Imaging with Immersion Technology at Albany NanoTech. B. Martinick, F. Goodwin, and Y. Wei (Infineon Technologies); R. Housley, P. Benson (Micron Technology); K. Cummings (ASML) International Symposium on Immersion Lithography, 2005
7. Immersion Defect Studies on the 1150i α-Tool. S. Brandl, Frank Goodwin, and Yayi Wei, (Infineon Technologies); P.Benson, R. Housley (Micron Technology); C. Robinson, D. Corlis (IBM); U. Okoroanyanwu (AMD); R. Watso, K.Cummings (ASML) International Symposium on Immersion Lithography, 2005
8. 193nm Immersion Material Top Coat Acid and Resist Photo Acid Generator Interaction. P. Benson, R. Housley (Micron Technology); F. Goodwin, Y. Wei (Infineon Technologies); N. Katchur, T. Tachikawa (OHKA America); K. Ohmori (Tokyo OHKA Kogyo)
9. Immersion Lithography Water Quality Learning at Albany. C. Robinson, D. Corliss (IBM); J.Barns, K. Cummings, H. Jansen, B. Lee, and R. Watso (ASML); J. Woodbeck (Albany NanoTech); F. Goodwin, B. Martinick, and Y.Wei (Infineon Technologies); P. Benson, R. Housley (Micron Technology); U. Okoroanyanwu (AMD)

Auxillary Ultra Pure DI Water Plant:

- **Anion and silica removal bed**
- **5.5 gpm pumps**
- **Heat exchanger**
- **UV radiation – oxidation**
- **Anion / Cation removal beds**
- **Dissolved gas removers (2)**
- **N_2 Regasifier (currently off)**
- **6000 MW polysulfone particle filter**
- **Inline Metrology**
  - **Resistivity / temp / flow**
  - **TOC**
  - **N_2/O_2 Dissolved gas**
  - **Particle (calibrated to >50nm)**
- **High purity sampling chamber**

Figure 1.

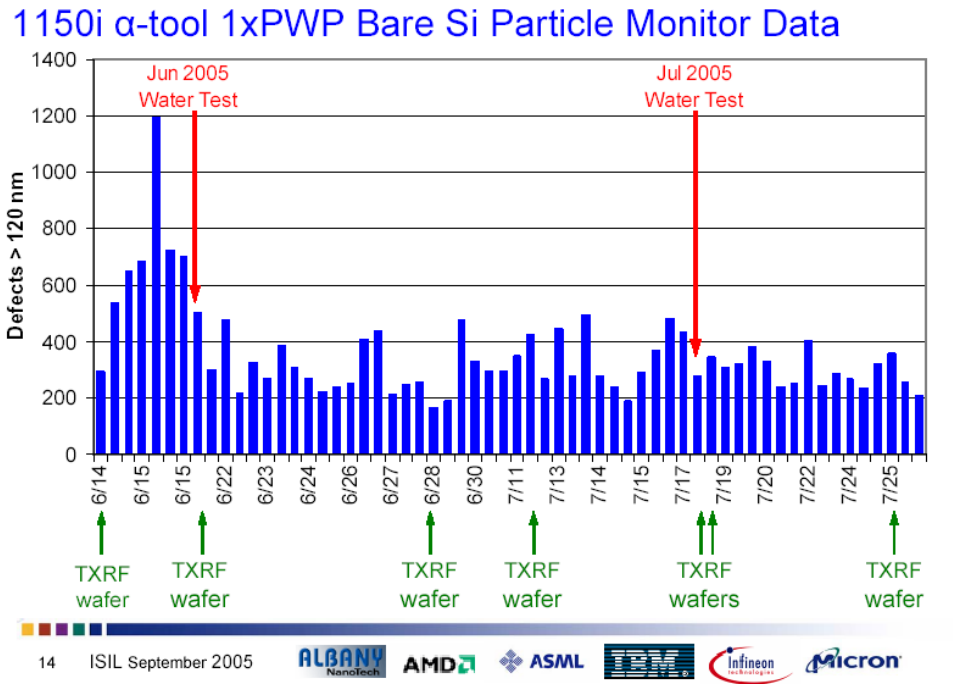
1150i α-tool 1xPWP Bare Si Particle Monitor Data
Defects > 120 nm
1400
1200
1000
800
600
400
200
0
Jun 2005
Water Test
Jul 2005
Water Test
6/14
6/15
6/15
6/22
6/23
6/24
6/26
6/27
6/28
6/30
7/11
7/13
7/14
7/15
7/17
7/19
7/20
7/22
7/24
7/25
TXRF wafer
TXRF wafer
TXRF wafer
TXRF wafer
TXRF wafers
TXRF wafer
14
ISIL September 2005
ALBANY NanoTech
AMD
ASML
IBM
Infineon
Micron

Figure 2.

SAMOS (straylight)

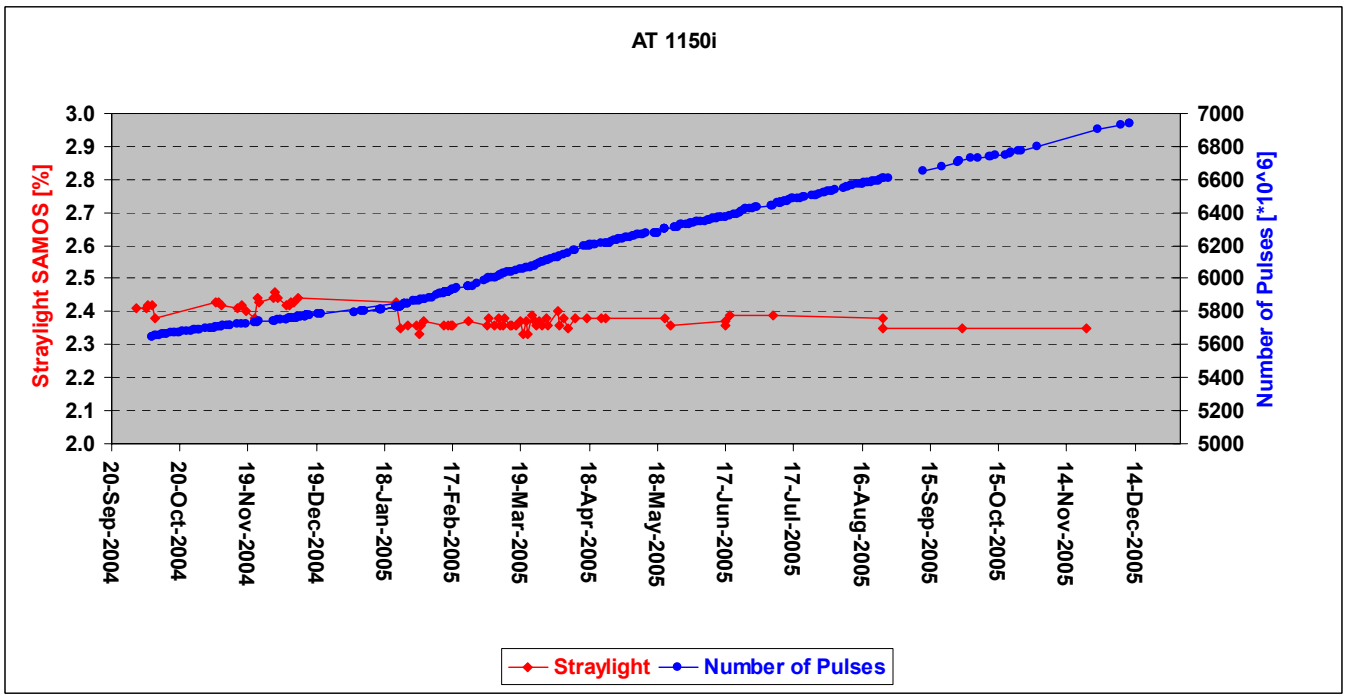

Figure 3.