EUVL System – Moving Towards Production

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ABSTRACT

Single exposure lithography is the most cost effective means of achieving critical level exposures, and extreme ultraviolet lithography (EUVL) is the technology that will enable this for 27nm production and below. ASML is actively engaged in the development of a multi generation production EUVL system platform that builds on TWINSCAN™ technology and the designs and experience gained from the build, maintenance, and use of the Alpha Demo Tools (ADTs). The ADTs are full field step-and-scan exposure systems for EUVL and are being used at two research centers for EUVL process development by more than 10 of the major semiconductor chip makers, along with all major suppliers of masks and resist. In this paper, we will present our EUVL roadmap, and the manufacturing status of the projection lens for our first production system. Included will also be some test data on the new reticle pods. Experimental results from ADT showing the progress in imaging (28 nm half pitch 1:1 lines/spaces CDU ~10%), single machine overlay down to 3 nm, and resist complete the paper.

Keywords: EUV lithography, system performance, sources, resist images, devices, high volume manufacturing.

1. INTRODUCTION AND ASML EUVL ROADMAP

The ASML Alpha Demo Tools (ADTs) are 0.25NA full field step-and-scan exposure systems for EUVL and are being used at IMEC in Leuven, Belgium and at the College of Nanoscale Science and Engineering at the University of Albany (Albany, NY) in the USA for EUVL process development. IMEC and Albany including their respective partners at present focus on EUV technology development including flare- and mask shadowing compensation, defect printability, and work on electrically active devices. Details of this work can be found elsewhere[1] - [3],[14] - [16].

ASML is taking the same modular design approach for the EUV platform (called the TWINSCAN NXE platform) as was done for our current state-of-the-art TWINSCAN™ platform: through a series of optics upgrades in a fixed body we plan to step through several technology nodes, all the way down to the 11nm half pitch node. A schematic of that EUV roadmap can be seen in Figure 1. The introductory system addresses the 27nm node and comprises a lens with the same 0.25 NA as the ADTs with significantly improved optics and enhanced illumination (variable coherence of 0.1 – 0.8). The 22nm high volume manufacturing node will be supported with a 0.32NA lens, and the 16nm node with the same NA lens, but with enhanced off-axis illumination modes. In addition, one can observe in our EUVL roadmap both single-machine overlay and productivity improvements. Section 3 will describe in more detail the required technical steps to support that roadmap.

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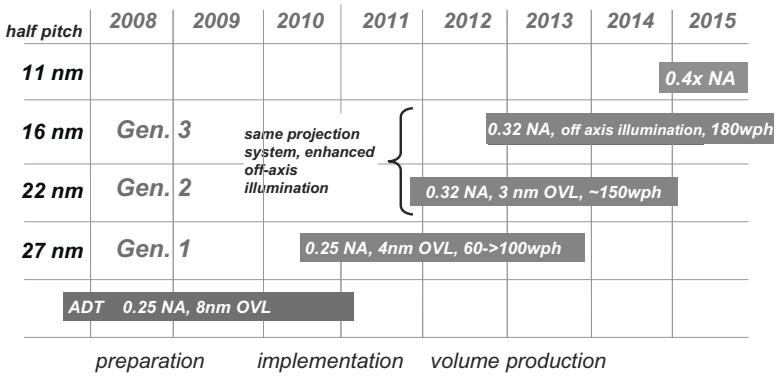


Figure 1. ASML's NXE platform development roadmap for EUVL.

Starting point for ASML's EUVL platform development are the ADTs. In the next section we will summarize its main accomplishments. In Section 3 we will describe in detail the NXE platform development, and in Section 4 the status of the EUVL infrastructure (including mask manufacturing and resist development).

2. EARLY PROCESS DEVELOPMENT USING ALPHA DEMO TOOLS

Details of the main specifications and hardware configuration of the ASML EUV ADT can be found elsewhere[4]-[11]. The ADT systems are equipped with a 0.25NA lens and a second generation Sn source. This second generation Sn source comprises a discharge produced plasma (DPP) Sn source from Philips Extreme UV GmbH, a debris mitigation system, and a grazing incidence collector from Media Lario Technologies. The next section summarizes some of the results obtained with this system configuration.

2.1. ADT Sn source and system productivity

A schematic overview of the ADT source can be seen in Figure 2 below. The EUV radiation is produced by an electric discharge through a small Sn cloud. Apart from EUV radiation, the Sn source produces out-of-band radiation, heat, and (fast) Sn debris. The Sn debris is filtered out by a foiltrap assembly - located in front of the grazing incidence multi-shell collector - that protects the collector optics from sputtering by fast Sn-ions/clusters and from reflection loss due to Sn (droplet) deposition. The collector projects an image of the plasma onto an intermediate focus aperture after which it enters the illuminator in the scanner. The heat that the source produces is dealt with through design and proper choice of materials. The front part of the foiltrap assembly can withstand 1500°C, whereas the non-13.5-nm radiation is either not collected by the collector or it is mostly filtered out by the multilayer coated EUV optical elements in the scanner.

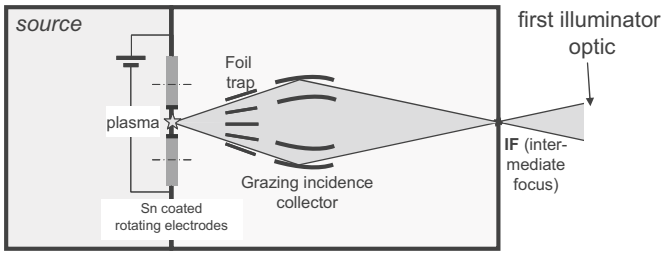


Figure 2. Schematic overview of the ADT Sn source.

Currently, both ADTs are equipped with a 120W source. The 120W nomenclature refers to the amount of in-band EUV radiation emitted by the plasma in a semi-sphere of 2π. Since the collector does not capture all the light emitted in 2π and since neither the debris mitigation system nor the collector have a 100% transmission, the amount of EUV light at intermediate focus is significantly lower.

For the 120W source an EUV output power of 5.3 W is determined, which is a ~10x improvement compared to the first generation Sn source. The more than ten fold output power increase for the 120W source has resulted in an equal power increase at wafer level. As a result, the ADT throughput capability has improved to >4 wafers per hour (w/h), determined at a resist sensitivity of 5 mJ/cm^2, as can be seen in Figure 3. This improvement is illustrated by the diamond-shaped symbols in Figure 3, where the progress in measured throughput for one of the ADTs is plotted. It can be seen that the current throughput can be up to 4.6 w/h. The triangles represent the in-band EUV power measured at wafer level. As can be seen in the right-hand side chart of Figure 3, between October 2007 and February 2009 close to 1200 300-mm wafers were exposed in the ADTs for R&D purposes.

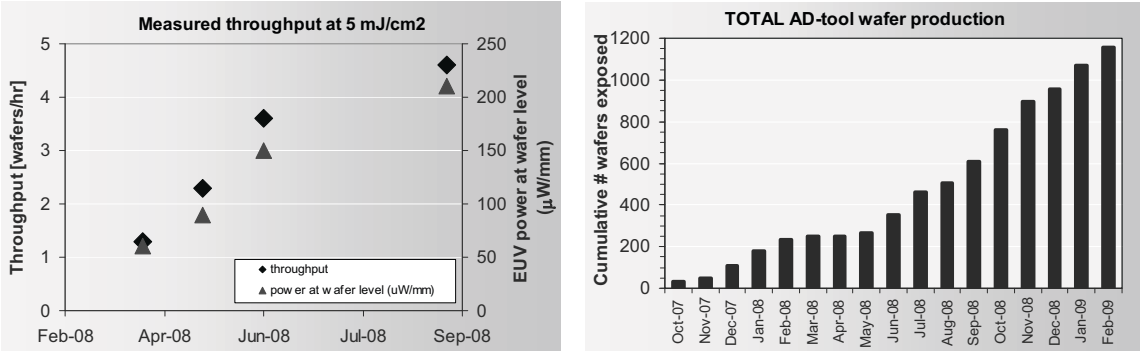


Figure 3. Left: measured throughput and power at wafer level *versus* time in one of the ADTs with a 120W source. Right: cumulative amount of wafers exposed in the ADTs - close to 1200 300-mm wafers for R&D were exposed so far.

In addition to the throughput, also the slit uniformity and its stability have notably improved with the installation of the 120W source. The improvement in the slit uniformity is illustrated in Figure 4, where champion data for one of the ADTs is plotted. Similar results are obtained on the other ADT. The improved slit uniformity originates from the better collectable pinch (more EUV in a smaller volume) and a slightly improved module alignment. As a result, the far-field image on the first illuminator mirror resembles more the originally anticipated far-field upon which the EUV illuminator optics was designed. The slit uniformity before Unicom correction improved and consequently the slit non-uniformity after Unicom improved from 3.2% to 0.95%.

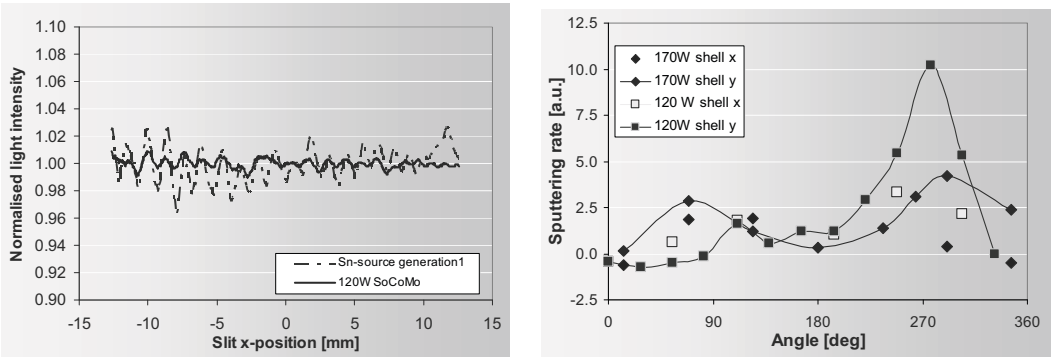


Figure 4. Left: champion data of slit uniformity with the first generation Sn source and the 120W source. Right: comparison of the angular dependence of the collector sputter rate in 120W and 170W source configurations for two shells x and y.

As the ADTs typically expose up to 1 GShot per month, source, foiltrap, and collector usage limitations are a serious concern. In the 120W source configuration, sputtering by fast ions was limiting the collector lifetime. Changes in the EUV reflective coating on the collector have yielded an almost ten-fold increase in lifetime, and changes in the foiltrap system have even further increased collector lifetime. The right-hand side graph in Figure 4 demonstrates the succesfull implementation of the improvements in the foiltrap system of the 170W source compared to the 120W source. The sputtering rate measured on witness samples is plotted as a function of angle around the circumference of the collector at

two different radii in the collector (*i.e.* at shell x and shell y). Design improvements have decreased the maximum sputtering rate of the 170W source by more than a factor of two compared to that of the 120W source. As a result of the above, the extrapolated collector lifetime meanwhile exceeds 35 GShot.

2.2. ADT single machine overlay performance

The overlay performance of the ADT has improved considerably over the last year. To determine single-machine overlay we expose 40 fields (field size: 26mm x 26mm) twice in MET-1K resist of RHEM, where each field contains a grid of 13x15 XPA alignment markers. After the wafer and reticle are removed from the system, a second exposure with the same reticle and wafer, which are re-loaded, is performed. The second exposure is shifted with a fixed offset in *x* and *y* compared to the first exposure. The overlay champion data histogram can be seen in the right-hand side of Figure 5. After applying mathematical corrections for the shift between the first and second exposure, the champion 99.7% single-machine overlay value amounts to 1.7 nm in *x* and 2.9 nm in *y* direction, respectively.

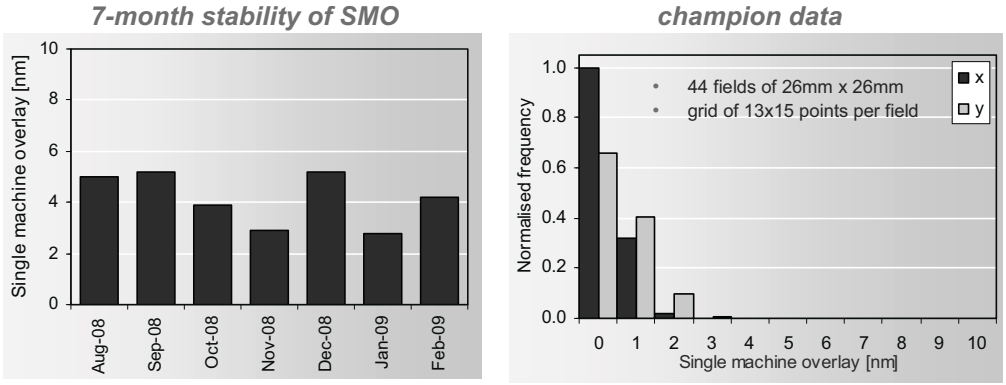


Figure 5. ADT single-machine overlay stability (left) and histogram of champion data (right).

On the left-hand side of Figure 5 the overlay performance improvement over time can be seen. Early last year we reported <8 nm overlay; currently it is consistently below 5 nm, with best result of 2.9 nm.

2.3. ADT vacuum reliability

We monitored the reliability of the vacuum in one of the ADTs. For a period of 49 weeks in 2008 we achieved an excellent vacuum uptime of 95.7% in the main chamber, which holds the illuminator and lens optics as well as the reticle stage and positioning- and vacuum metrology. As can be seen in Figure 6, in that 49-week period we had only one vacuum hardware related down, due to failure of a more than three year old prepump.

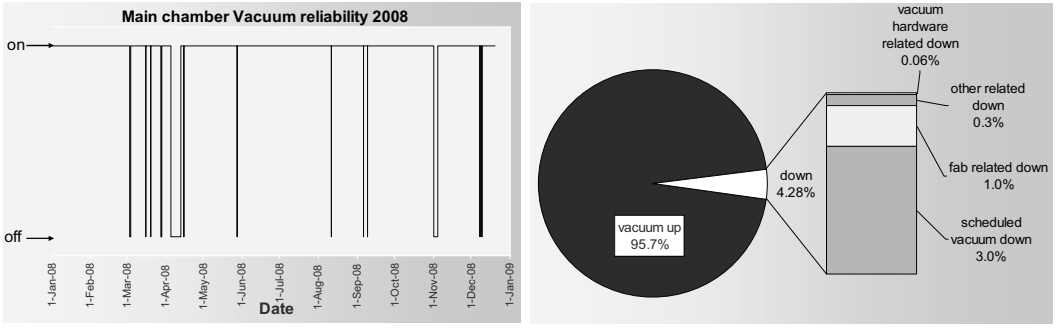


Figure 6. Vacuum reliability of the ADTs is high; the uptime of the main chamber (including optics and stages) exceeds 95%, measured over a 49-week period (total: 8232 hrs).

It confirms that EUV vacuum lithography can be achieved in a reliable way.

2.4. ADT imaging results

This section provides a summary of some of the key imaging data that has been collected from the ADTs. More details of this work can be found elsewhere[12].

2.4.1. Resolution limit full field 1:1 L/S imaging

The imaging performance of the ADTs has been studied by looking at a number of features. First the baseline tool performance is determined by simulating exposure latitude - defined as 10xNILS in resist to mimic a perfect resist (zero acid diffusion length) - *versus* pitch. The contrast loss from the exposure tool is estimated by including 1.2nm RMS lens aberrations (Z5-Z36), 1.6% DC flare (which is an estimate of the specified 16% flare of the entire point spread function under a 2 micron line in combination with a 90% dark field reticle), 2nm Moving Standard Deviation for stage vibrations in horizontal direction and 20nm in vertical direction. Figure 7 shows that the theoretical resolution limit for the ADT's is 20nm half pitch. However, if we take 10% EL as the minimum requirement to resolve a pattern in resist, then the resolution limit is 25-26nm half pitch. Last year, a resolution of 28nm 1:1 L/S was demonstrated on ADT[13], and recently even 26 nm[15]. Also recently, the CD uniformity of 28 nm hp 1:1 L/S was determined to be 3.0 nm (3σ) for horizontal and 2.2 nm (3σ) for vertical lines. Details of this can be found elsewhere[14]. Further improvements in the resist contrast are expected to bring the resolution further down to ~25nm half pitch.

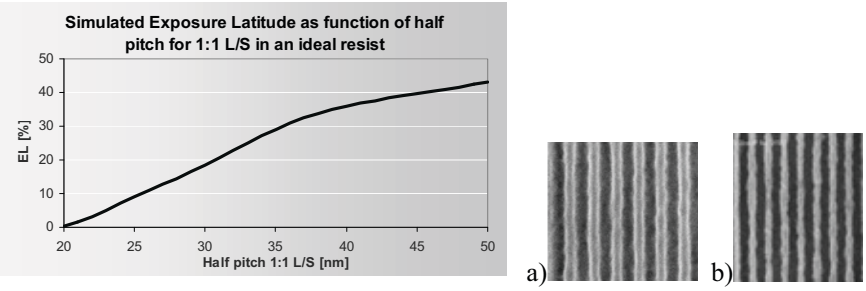


Figure 7. Left: Simulated exposure latitude as function of half pitch in an ideal resist. Right: a) 28nm[13], ; and b) 26nm[15] 1:1 L/S imaging demonstrated on ADT.

2.4.2. Process window evaluation L/S imaging at 28 nm half pitch

CD uniformity was measured for the 28nm half pitch NAND Flash gate layer modules on our test mask. The exposure recipe contains 39 full fields (26.5 x 32.5 mm^2) distributed across the wafer, of which 23 are exposed at nominal energy and nominal focus, and the remaining 16 are exposed at nominal energy and with a focus offset between -120 and +120nm (*i.e.*, 8 additional focus levels with 30nm intervals and 2 fields per focus step). The measured vertical gate pattern is shown schematically in Figure 8 below, the horizontal patterns were measured as well.

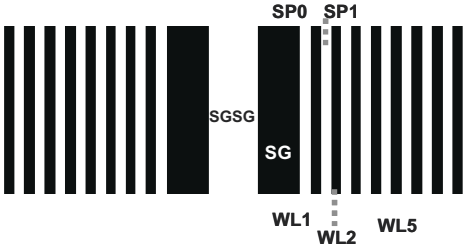


Figure 8. Schematic representation of the word line/gate layer and the features that are evaluated. Space SGSG is designed as 4x the word line half pitch, select transistor SG as 2.5x the word line half pitch, spaces SP0 and SP1 both have the word line half pitch, just like word lines 1, 2, and 5.

The CD uniformity requirement for 28nm NAND Flash according to the 2008 ITRS roadmap[17] is 2.9 nm 3σ for full lot CD control, including all lithographic error sources such as masks, resist, imperfect OPC, and exposure tool. Since the presented data is from a single wafer, the required CD control is tightened to 7.1% of the CD node, *i.e.* 2.0 nm 3σ for 28nm design rule, to judge the current performance against the final requirements. Figure 9 below shows the mean CD data, full wafer and intrafield CD uniformity for all measured word lines and spaces in the gate layer with 28nm half pitch design rule. The wafer was slightly underexposed, resulting in a mean CD of ~30nm for the wordlines and ~26nm for the spaces. The resist process has difficulties to clear out the spaces completely at these small feature sizes, which results in a larger CDU of the spaces, falling outside the 2.9nm ITRS requirement. The word lines, however, meet the ITSR requirement, or even meet our more stringent 7.1%-of-CD criterion. The pooled full wafer CDU of the word lines is 2.7 nm 3σ, indicating good CD control across the wafer, no asymmetry effects due to aberrations, and no proximity effects between word line 1, 2, and 5. It should be noted that no OPC was applied to any of the features on the mask, the shadow error through slit was not corrected, and no reticle error correction was applied. The horizontal features were biased on the mask with ~ -1.5nm (at wafer level) with respect to the vertical features..

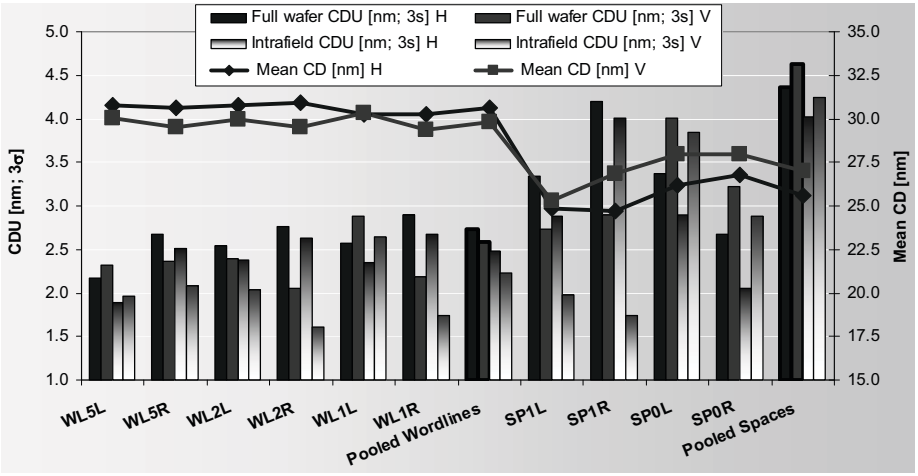


Figure 9. Mean CD, full wafer and intrafield CD uniformity for all evaluated word lines and spaces in the gate layer, both left (L) and right (R) of the central space (SGSG), for 28nm half pitch design rule. The pooled word lines meet the 2.9 nm CDU requirement in the ITRS.

Figure 10 shows CD SEM pictures of both the horizontal and vertical features from the 28nm Flash modules across the exposure slit. Some scumming and bridging is visible in the pictures, indicating that the process needs to be further optimized for 28nm half pitch and below. However, it is clear that the exposure tool is capable of resolving both horizontal and vertical 28nm Flash features across the slit in a single exposure with good uniformity.

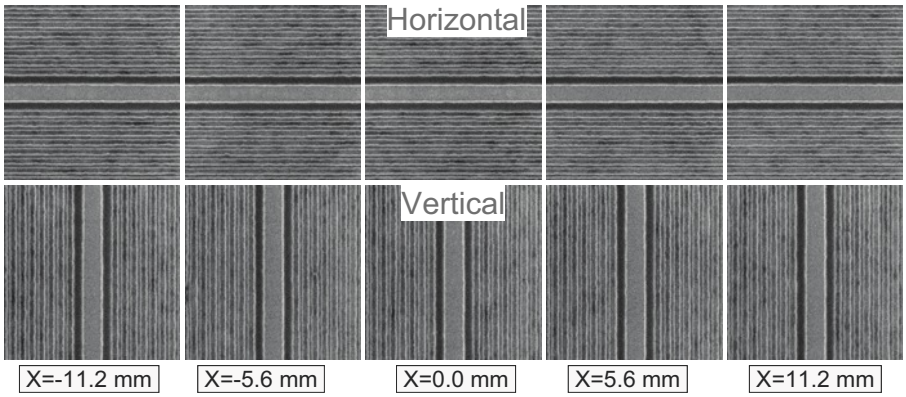


Figure 10. CD SEM pictures from the 28nm half pitch Flash modules across the exposure slit.

Figure 11 shows the measured Bossung curves for 28nm WL1 and SP0 exposed with EUV (NA=0.25, σ=0.5) compared to 40nm WL1 and 60nm SP0, which are the most critical features in the design, exposed with ArF immersion (NA=1.35, σ=0.82/0.97 dipole-X with 35^o opening angle, Y-polarized). The difference in DoF and focus sensitivity is obvious. In case of ArF immersion, the space between the first word line and the select gate (SP0) had to be biased to 1.5 x the word line half pitch (or more) to get sufficient process latitude. This is not necessary with EUVL, due to the much higher k_1 – value of 0.52 *vs*. 0.28.

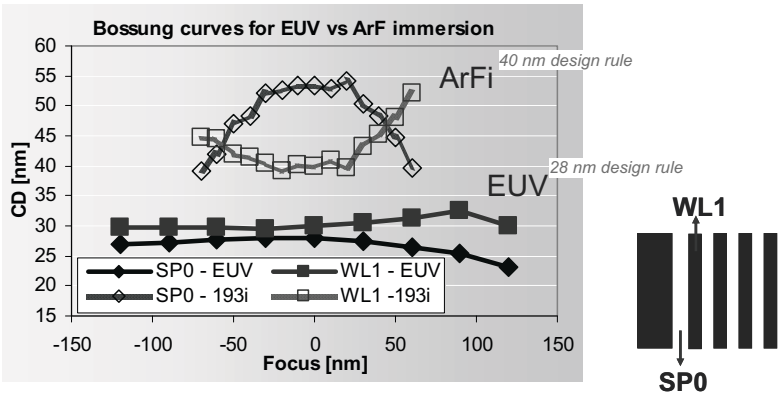


Figure 11. Bossungs curves for 28nm WL1 and SP0 with EUV (NA=0.25, σ=0.5) compared to 40nm WL1 and 60nm SP0 with ArF immersion (NA=1.35, σ=0.82/0.97 dipole-X with 35^o opening angle, Y-polarized)..

2.4.3. Contact hole imaging

Another main advantage of EUVL is the superior contact hole printing, especially of random contact hole applications. As an example, we present the process window of an SRAM-like contact hole pattern.

Our test mask contains an SRAM-like CH pattern with a 90nm minimum pitch (see Figure 12 below). Process windows for 8 contacts within the SRAM cell were measured to look at differences in process latitude and OPE within the cell. Unfortunately the dose targeting was not done correctly which resulted in severely underexposed CHs of less than 30nm. However, even at these unfavorable conditions, the contact holes are well defined, were resolved over 200nm focus range, and showed no appreciable CD variation between the holes within the cell (< 1.2 nm, see Figure 12). No OPC on the mask was applied to this CH pattern. Figure 12 also shows the ellipticity, defined as the ratio between the long axis and the short axis of the CH, for the 8 evaluated holes. The ellipticity was found to be 1.1 on average, with the long axis (almost) parallel to the horizontal axis. This means that the width of the CHs is ~3nm larger than their height, consistent with mask shadowing.

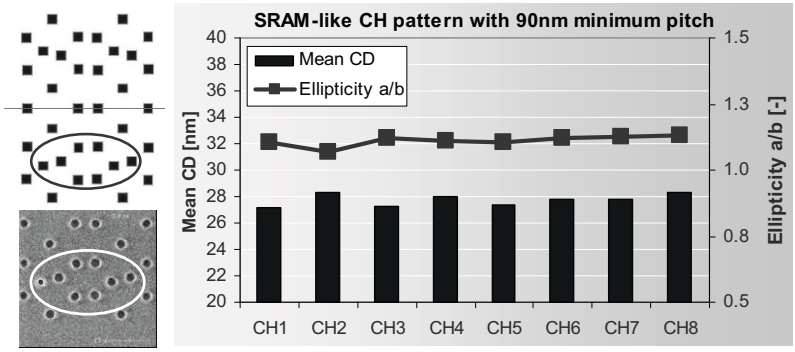


Figure 12. Left: SRAM CH pattern on our test mask and CD-SEM picture of the CHs in best focus. Process windows were measured for the 8 contacts in the encircled area. Right: Measured mean CD and ellipticity of the 8 evaluated CHs.

2.4.4. Device performance using EUVL from the ADTs

With all the knowledge gained over the years the ADT customers have been able to incorporate EUV-exposed layers in existing device fabrication process flows. Last year, both IMEC and the Albany organisation showed electrically functioning devices, as summarized in Figure 13. Details of this work can be found elsewhere[1],[3].

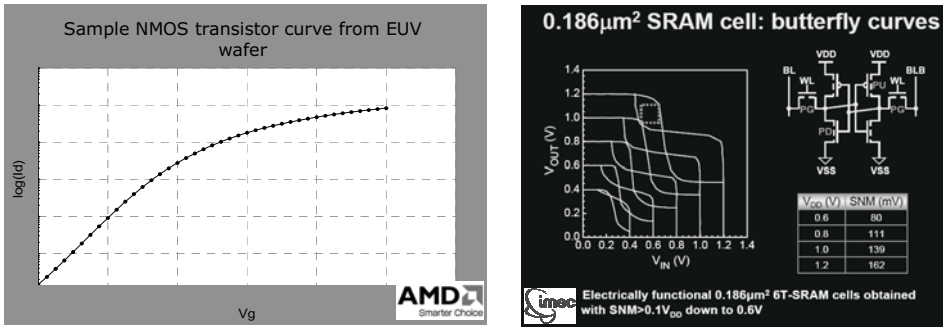


Figure 13. Left: electrically functioning transistor of which the first metal level was exposed on ADT[1]. Right: electrically functional 0.186 μm^2 6T-SRAM cell, of which the contact hole layer was exposed on ADT[3].

Work is in progress to demonstrate functional 22nm SRAM test devices of which one or more metal/contact layers are exposed using EUVL.

3. NXE PLATFORM FOR HIGH-VOLUME MANUFACTURING

3.1. Exposure system development: status and plans

As in the past for 200mm and 300mm optical lithography, ASML introduced a new high-productivity platform for EUVL that is capable to support multiple technology nodes. Table 1 below lists an overview of the main specifications and configuration choices of the NXE platform from 2010 to 2012, detailing out the roadmap as shown in Figure 1. Over the years the platform productivity will be enhanced from 60wph initially to 180wph. Enabler for this is the source development, which will be further explained lateron in this paper. Note that for 16nm resolution a resist dose of 15 mJ/cm^2 is assumed.

Table 1. Main ASML EUV platform (TWINSCAN NXE) specifications.

		2010	2011	2012
Resolution (HP)	nm	27	22	16
Lens NA		0.25	0.32	0.32
k1 factor		0.50	0.52	0.38
Illuminator		conv.	conv.	OAI
Overlay	nm	4.5	3.5	3.0
Productivity	wph	60	150	180
Resist Dose	mJ/cm^2	10	10	15

The NXE platform will be introduced in 2010 for the 27nm node, which is supported by 0.25NA optics with conventional illumination. This puts the k-factor to ~0.5, so into a regime where single exposures with little or no optical proximity correction (OPC) has to be applied. By enhancing the NA to 0.32 and adding off axis illumination the resolution can be extended to 16nm. In accordance with resolution, overlay and focus will be improved as well. From Figure 14 it can be deduced that with quasar illumination we can support the 16nm node, using an NA of 0.32, whereas with dipole illumination even 13nm can be resolved - with a NILS of >2.

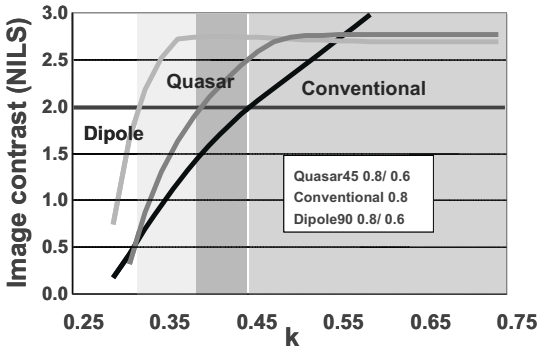


Figure 14. Image contrast as function of the k1-factor, using a 0.32NA lens.

The long term roadmap towards 11nm and even beyond will see higher NA optics. A few design examples are depicted in Figure 15. In addition, processes capable of a k-factor below 0.4 are required: resist performance needs to be improved in order to achieve a resolution significantly below 16nm. Main parameter is the acid diffusion length.

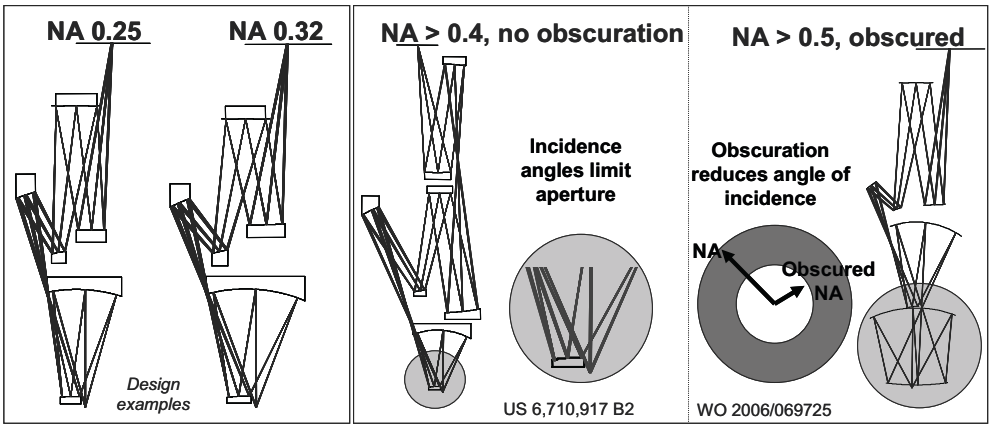


Figure 15. Possible optics design roadmap down to 11nm resolution with >0.4NA optics. All four diagrams are design examples.

3.2. Optics fabrication

Carl Zeiss SMT AG is currently manufacturing several sets of illumination and 0.25NA lens optics for the first systems of ASML's new NXE platform. There are significant performance improvements compared to the ADT optics that enable a resolution limit well below 27 nm for these tools. The illumination system has an increased (variable) partial coherence of 0.8. The lens is characterized by smaller wavefront aberrations (about 0.8 nm RMS) and a flare level well below 8%. In addition, the transmission of the complete optical train is improved by implementing mirror coatings with significantly higher reflectivity compared to the ADTs. The most prominent performance improvement is the flare reduction of the lens. Figure 16 shows the improvements in mid-spatial frequency roughness (MSFR) mirror polishing results over time. The ADT systems have a <16% flare level, based on an average MSFR of ~0.20 nm per mirror. For the first NXE systems we have manufactured more than 20 mirrors which support the 8% flare specification. In parallel, we focus on further flare reduction and process transfer for later (higher NA) optical systems. For that, we have recently finalized a test mirror with an MSFR of 0.068 nm RMS. This mirror fullfils all current performance targets. The flare contribution of such a mirror would be ¼ of what is currently required for the first NXE systems.

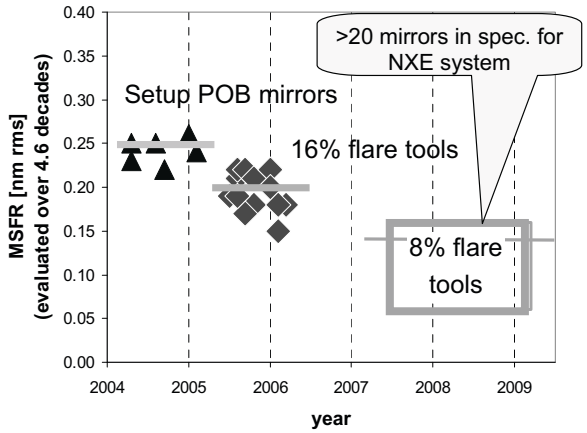


Figure 16. Progress in mirror polishing (MSFR), supporting <8% flare performance.

After having reached the roughness requirements the mirrors are coated with a Mo/Si multilayer stack. Here we have achieved significant reflectivity improvements compared to the ADT systems; the ADT mirrors have an average 64% peak reflectivity, whereas for the NXE mirrors we currently achieve up to 69% reflectivity. As we have six mirrors in the lens this results in nearly 50% increased transmission. The coating effort is supported by our partners - FOM Rijnhuizen, IWS institute, and IOF institute. The coating impact on non-correctable wavefront error currently adds about 0.030 nm per mirror to the wavefront performance of the optical system. This is a result of careful thickness control and a low coating stress of about 100 MPa.

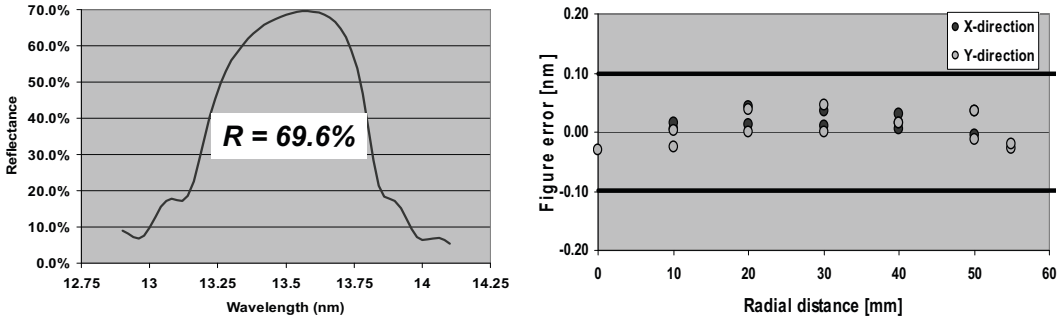


Figure 17. Left: mirror coating development for NXE has yielded >69% peak reflectivity. Right: added figure error due to the coating process for various lateral positions on the mirror.

All NXE lenses will be qualified with in-house EUVL wavefront metrology at Zeiss SMT. The metrology system is ready for qualification of the lens. On our teststand we have achieved a reproducibility of the individual Zernike aberrations close to or better than 0.1 nm. The availability of actinic wavelength metrology is a major milestone to qualify and guarantee a wavefront performance of the systems well below 1 nm.

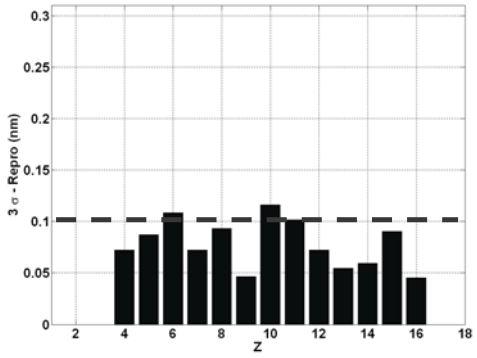


Figure 18. Aberration reproducibility versus Zernike number at the Zeiss actinic metrology test stand. Dotted line represents the requirement.

3.3. Sources for high-volume manufacturing

One of the critical needs for EUVL to be successful is high productivity, with the main criteria for this being high wafer throughput. Since EUVL is a photon limited technology, available source power is what drives overall system throughput. Regardless of source type, the main challenges for an EUV source are high power that is spectrally pure and maintains high output over a long period of time. These three challenges directly impact productivity, imaging, and cost of ownership (CoO).

There are two main types of EUV sources being developed for EUVL production systems – Discharge Produced Plasma (DPP) sources and Laser Produced Plasma (LPP) sources – for achieving these requirements , and the key elements of each are shown in Figure 19.

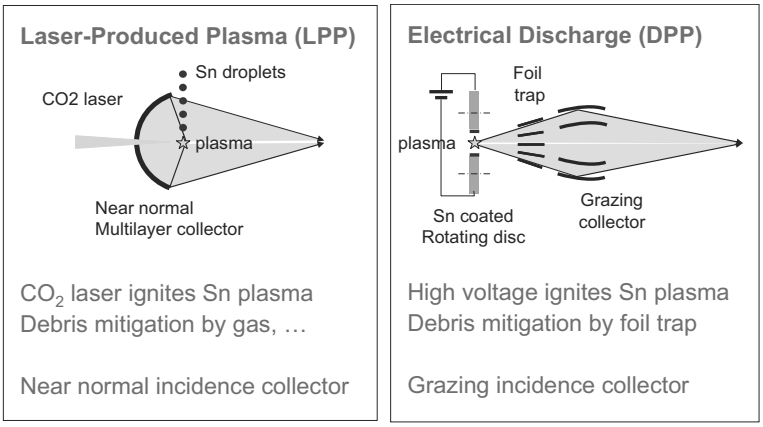


Figure 19. Key elements of sources for high volume manufacturing: LPP (left) and DPP (right).

For the first NXE systems an LPP source from Cymer is being developed, with a first generation capable of supporting 60 wph, and a roadmap of upgrades and development to support the ASML platform throughput roadmap of >100 300mm wph. Data has been collected from Cymer development sources demonstrating significant progress towards debris mitigation and exposure power, see Figure 20. Details can be found elsewhere[18].

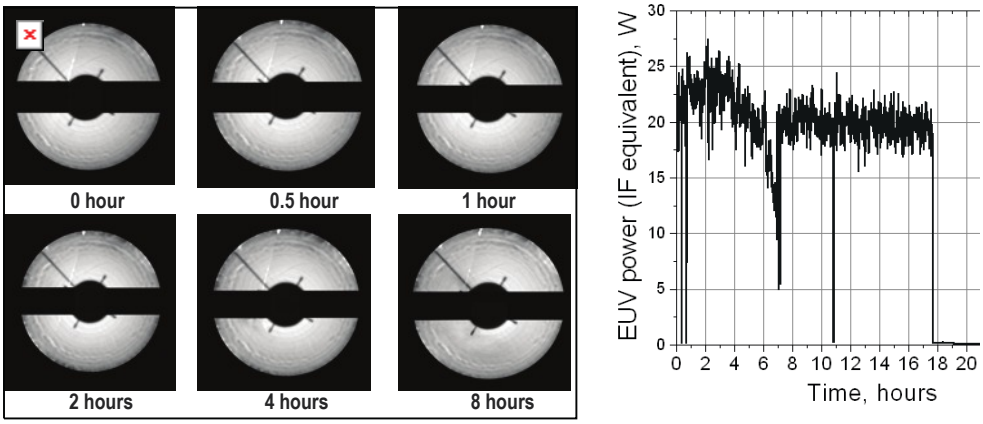


Figure 20. Left: 8hr endurance test of Cymer LPP source using fluorescent screen at the output of the source to evaluate the far-field distribution: no degradation of the images is visible, indicating that debris mitigation is functioning well. Right: 18hr source endurance test without a collector present – calculated (using a 5sr collector with 50% average reflectivity and 90% source module transmission) to have >20W in-band EUV power as output[18].

More development is needed to reach the full requirements for high volume EUVL, and all source suppliers are actively engaged in development activities aligned with these requirements.

4. PROGRESS IN THE INFRASTRUCTURE DEVELOPMENT FOR EUVL

To utilize EUVL in production, masks and resist have critical requirements to meet so that the 27nm node and beyond performance can be realized. For masks, the key specifications unique to EUV are mask flatness, bow, and defect density, while for resist, getting a fast resist with the necessary resolution and linewidth roughness (LWR) is key. The roadmaps in Figure 21 illustrate the timing needed for these key mask and resist requirements in order for chip manufacturers to realize in production the full capability of the NXE platform.

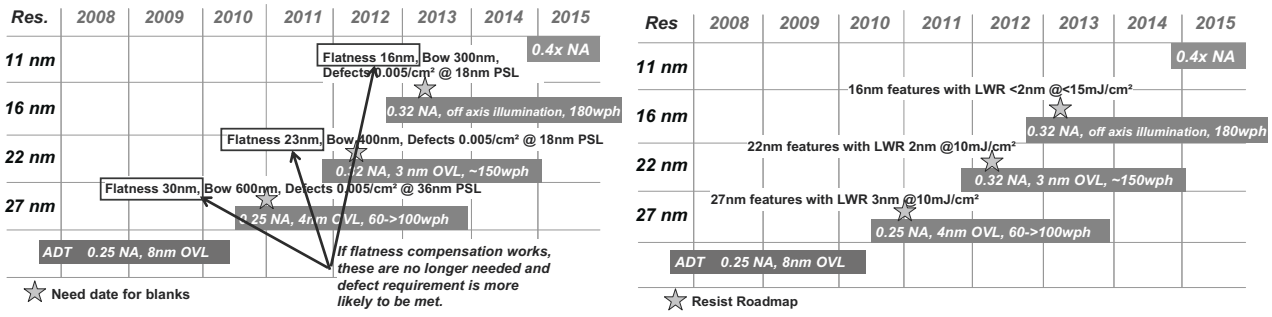
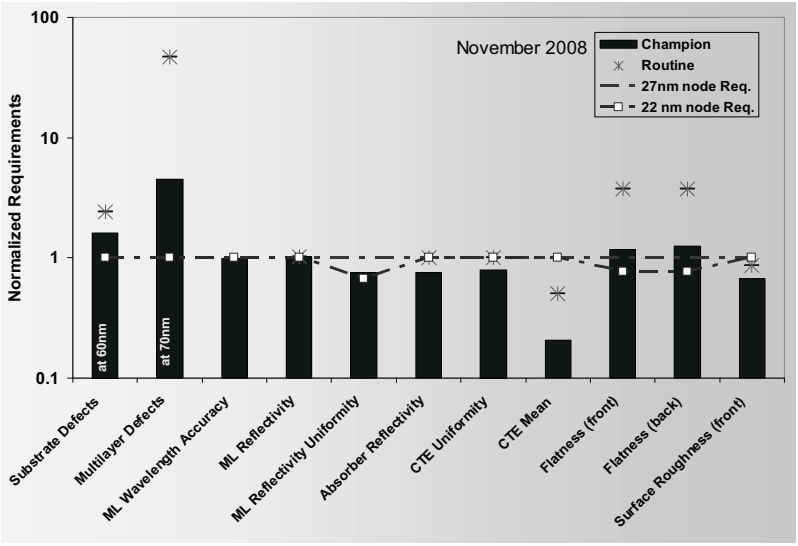


Figure 21. Roadmaps for mask (left) and resist technology (right).

4.1. Mask fabrication

EUV masks in form and function are the same as those for 193nm and 248nm, but there are some fundamental differences that drive the need for further optimization to the mask blank infrastructure. EUV masks, like the optics in the system, are reflective, and have a complex multilayer coating to optimize mask reflectivity. Since the writing of sub-30nm lithographic features is a common challenge for all mask technologies, we have concentrated on identifying the critical mask blank requirements needed for production of 27nm and 22nm devices with EUVL, building on items identified in SEMI Standards SEMI P38-1103 and P37-1102 and the pending P37 revision. In Figure 22 champion data and some routine data of mask blanks is compared against the 27nm and 22nm production requirements. Bars greater

than 1 in the chart indicate mask blank parameters that need improvement. The two biggest challenges facing mask blank suppliers are defects and flatness requirements.



EUV Mask Parameter	Lithography Impact
Substrate Defects	Yield
Multilayer Defects	Yield
ML Wavelength Accuracy	Throughput
Reflectivity	Throughput
Reflectivity (uniformity)	CDU
Absorber Reflectivity	Contrast
CTE Uniformity	Overlay
CTE Mean	Overlay

Figure 22. Status of key requirements of mask blank fabrication, and their impact on lithographic performance.

In Figure 23 we show champion defect data for blanks. From the bars in this chart we see that the defect density goes up as the metrology resolution (bullet symbols) decreases, but then usually process improvements are made which reduce the defect density at that inspection size. These results highlight the importance of metrology in enabling the mask blank suppliers reaching the necessary defect density levels.

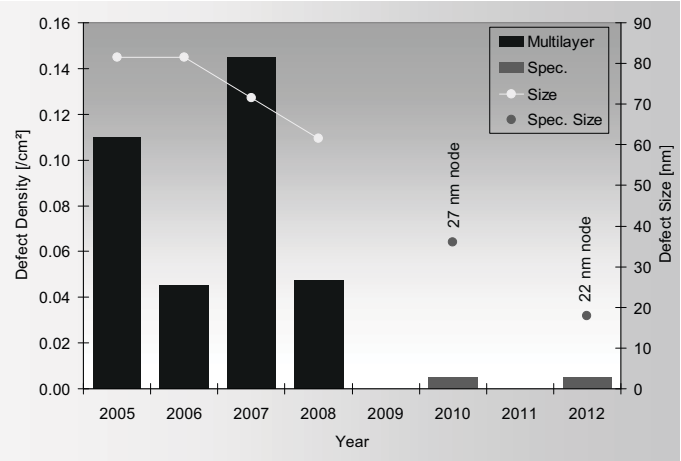


Figure 23. Progress in defect density reduction together with improvements in metrology/inspection size.

4.2. Defect-free mask handling

EUV masks will not have a traditional pellicle for protection, thus the EUV reticle carrier with inner pod will accomplish defect-free protection for the mask. ASML has focused on the standardization of the carrier and inner pod, and has enabled the design and fabrication of reticle carriers compliant with the newly created SEMI Standards. Figure 24 is a photograph of the prototype carrier and inner pod. This assembly was tested for reticle transport, and <0.9 added defects of size >53 nm per roundtrip shipment (fab, truck, plane, truck, fab) were determined.

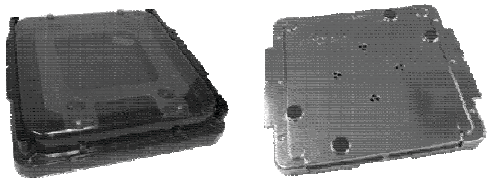


Figure 24. Photograph of mask carrier (left) and inner pod (right).

The carrier and inner pod have also been tested to show protection of the mask as it might be handled in a lithography tool. In the NXE system, only the inner pod with the reticle will be transferred through the load-lock from atmosphere to vacuum. The front- and backside of the reticle are covered at all times in the vacuum system, except when the reticle is brought to the reticle stage for exposure. To mimic use in the system, we tested a simplified reticle handling cycle from carrier to pumping and venting of the inner pod in the load lock, and inner pod cover removal and placement cycling in vacuum. As shown in Table 2, the prototype carrier and inner pod had no particles added during any of these tests.

Table 2. Results of particle testing inside the exposure system.

Test	Cycles	Adders per cycle, 53nm particle size
Complete handling from carrier to cover removal	370	0.00
Pump and vent in the load lock	60	0.0
Inner pod open / close of cover	1100	0.000

Work is in progress to evaluate the complete reticle handling sequence, including scanning of the reticle stage.

4.3. Resist development

As with every new litho generation, EUV resists must go through optimization, balancing the need for resolution, LWR, and dose. EUVL has the benefit that the chemically amplified resists used in 248nm and 193nm can also be used, as has already been illustrated with the excellent imaging on ADT. Based on champion results over recent years, we have summarized in Figure 25 imaging results at three different dose levels. For each of the three dose levels, we have extrapolated the trend to see the progress being made towards the production requirements for 27nm, 22nm, and 16nm lithography. To maintain maximum NXE productivity, at the currently planned source power level a dose sensitivity of 10 mJ/cm^2 is needed for 27nm and 22nm, and 15 mJ/cm^2 is needed for 16nm and below. As can been seen from Figure 25, progress in the near term appears adequate for 27nm and even 22nm, but will need acceleration beyond that. Use of the ADTs the coming years will be a critical enabler for resist suppliers achieving the required improvements.

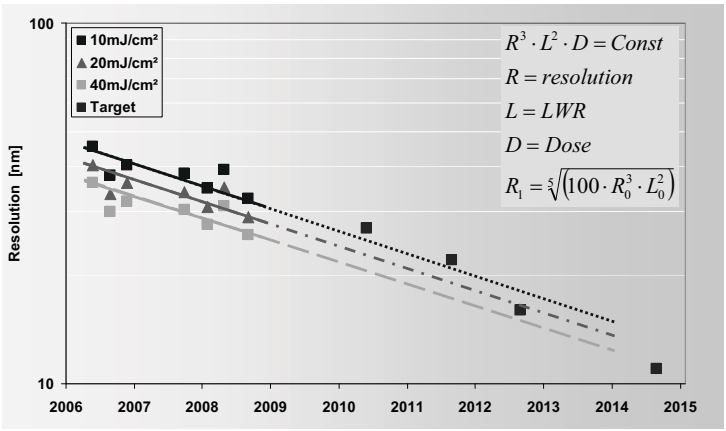


Figure 25. Resolution progress as a function of dose. All data scaled to 10% LWR.

5. SUMMARY AND CONCLUSIONS

ASML has presented its EUVL realization roadmap. Platform development supports imaging down to the 16 nm node through a series of improvements in optics, overlay, and productivity. On ADT a CD uniformity of ~10% for 28 nm half-pitch dense lines/spaces was determined. Although resist development progress for the 27nm and 22nm device production appears adequate, more progress is needed to support imaging at high productivity below 22nm half pitch.

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